A Maxim Integrated Products Brand

PHY1071-01

125Mbps – 2.125Gbps VCSEL Driver / Post amp with Digital Diagnostics

Features

- Multi-rate from 125Mbps to 2.125Gbps
- VCSEL driver output stage with 16mA max modulation drive and 20mA bias current
- Programmable mean power control loop
- Temperature compensated modulation current
- Integrated limiting amplifier with selectable swing CML output to reduce radiated emissions
- Programmable receiver low pass filter
- Integrated Loss Of Signal function
- Digital diagnostic mode compliant with SFF-8472 using an external MCU
- Stand-alone mode where device parameters are loaded from an external EEPROM
- -40°C to +85°C operating range
- 36pin 6mm x 6mm QFN package
- Eye safety logic

Applications

- SONET, Fibre Channel, GbE
- SFF and SFP Modules

Description

The PHY1071-01 is a combined VCSEL driver and limiting amplifier with support for Digital Diagnostic Monitoring for use within small form factor modules for Fibre Channel applications.

The transmitter integrates a high speed output stage with programmable bias and modulation currents, controlled through a 2-wire serial interface. The mean power control loop allows connection in both common cathode and common anode configurations.

A Loss Of Signal (LOS) detector is included with detection based on either the receiver photo detector average current or received signal modulation amplitude.

When used in digital diagnostics mode the integrated A/D converters measuring temperature, TX Bias, Supply Voltage, RX Signal Strength and Mean Power are read via a 2-wire serial interface. An external Microcontroller Unit (MCU) is used for calibrating real time diagnostic monitors and alarm generation.

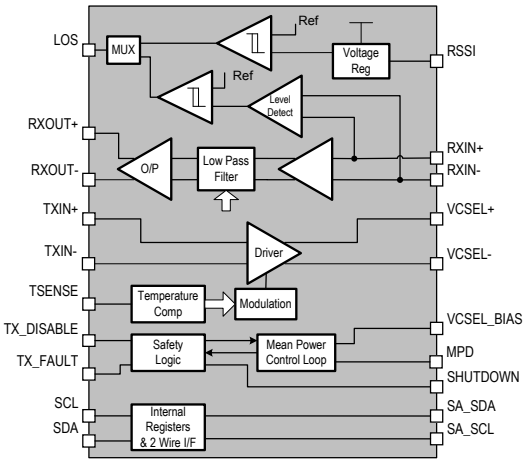


Figure 1 - Outline Block Diagram

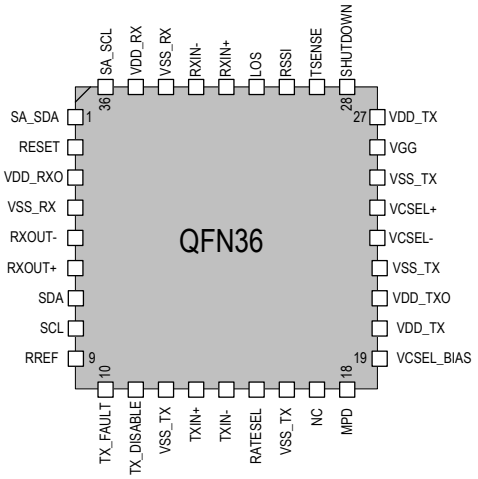


Figure 2 - Device Pin Out (Top View)

Table of Contents

1. Ordering Information

Part Number	Description	Package
PHY1071-01QD-RR	Enhanced 2G VCSEL driver and Post Amp	QFN36, 6mmx6mm in Tape and Reel, RoHS compliant *(see Figure 43, p. 47)*
PHY1071-01QS-RR NOT FOR USE IN NEW DESIGNS	Enhanced 2G VCSEL driver and Post Amp	QFN36, 6mmx6mm in Tape and Reel, RoHS compliant *(see Figure 43, p. 47)*

2. Pin Description

Pin No	Name	Direction	Type	Description
1	SA_SDA[1,4]	I/O	LVTTL	2-wire serial interface. Connects to EEPROM in stand alone mode
2	RESET	I/P	CMOS	Reset
3	VDD_RXO[2]		Power	Limiting amplifier output power supply
4	VSS_RX[3]		Ground	Receiver section ground connection
5	RXOUT-	O/P	CML	Limiting amplifier differential serial data output.
6	RXOUT+	O/P	CML	Limiting amplifier differential serial data output.
7	SDA[4]	I/O	LVTTL	2-wire serial data interface. Used in Digital Diagnostics Mode.
8	SCL[4]	I/P	LVTTL	2-wire serial interface clock. Used in Digital Diagnostics Mode.
9	RREF	I/P	Analog	Connect to Ground through a 10k resistor
10	TX_FAULT	O/P	LVTTL (open collector)	Transmit fail alarm. A logic 1 indicates a fault in the transmission system. Requires external pull up for SFP MSA compliance
11	TX_DISABLE[4]	I/P	LVTTL	Output disable (active high). Disables VCSEL drive. On chip 8k pull up
12	VSS_TX[3]		Ground	Transmission circuitry ground connection
13	TXIN+	I/P	CML	Differential VCSEL driver input from host
14	TXIN-	I/P	CML	Differential VCSEL driver input from host
15	RATESEL	I/P	LVTTL	Toggles between two low pass filter characteristics. External 30k pull down resistor required for SFP MSA compliance
16	VSS_TX[3]		Ground	Transmission circuitry ground connection
17	NC			No connection. Leave open circuit
18	MPD	I/P	Analog	Monitor photodiode input
19	VCSEL_BIAS	O/P	Analog	VCSEL bias current output
20	VDD_TX[2]		Power	Transmission circuitry power supply connection

21	VDD_TXO[2]		Power	Transmission circuitry power supply connection
22	VSS_TX[3]		Ground	Transmission circuitry ground connection
23	VCSEL-	O/P	High speed	VCSEL differential driver output
24	VCSEL+	O/P	High speed	VCSEL differential driver output
25	VSS_TX[3]		Ground	Transmission circuitry ground connection
26	VGG		Ground	Ground substrate connection
27	VDD_TX[2]		Power	Transmission circuitry power supply connection
28	SHUTDOWN	O/P	CMOS	Gate drive for optional VCSEL shutdown FET switch
29	TSENSE	I/P	Analog	External temperature sensing transistor connection
30	RSSI	I/P	Analog	Receive signal strength indicator & regulated supply for Rx photodiode
31	LOS	O/P	LVTTL (open collector)	Loss of signal output. Requires external pull up for SFP MSA compliance
32	RXIN+	I/P	CML	Limiting amplifier differential serial data input
33	RXIN-	I/P	CML	Limiting amplifier differential serial data input
34	VSS_RX[3]		Ground	Receiver ground connection
35	VDD_RX[2]		Power	Limiting amp power supply
36	SA_SCL[1,4]	I/P	LVTTL	EEPROM 2-wire serial interface clock
-	PADDLE		Ground	Ground / Thermal Paddle

1 Used in stand-alone mode only.
2 All VDDs are internally connected by back-to-back protection diodes. VDDs should not be powered up independently.
3 All VSSs are internally connected to the IC substrate connection.
4 Internally pulled high with an 8kΩ pull-up resistor.

3. Key Specifications

3.1. Absolute Maximum Ratings

Parameter	Conditions	Min	Typ	Max	Unit
Supply Voltage		- 0.5		+6.5	V
Voltage on any pin		VSS - 0.5		VDD + 0.5	V
Storage Temperature				150	°C
Soldering Temperature	For 25 seconds			260	°C
Junction Temperature				140	°C
ESD	Human Body Model	2			kV

Under absolute maximum rating conditions device not guaranteed to meet specifications; permanent damage may be incurred by operating beyond these limits.

3.2. Continuous Ratings

Parameter	Conditions	Min	Typ	Max	Unit
Operating Supply Voltage	Continuous operation	2.97	3.3	3.63	V
Current consumption	Excluding bias & modulation at 10mA bias & 8mA modulation			102	mA
Operating temperature	Ambient Still Air, Max Bias and Modulation Current	-40	25	+85	°C

3.3. Receiver

3.3.1. Receive Limiting Amplifier

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Sensitivity		Differential, BER=1*10^{-12} <2.125Gbps		5	7.5	mVpp
Max Differential Input		Overshoot and TJ within spec	1200			mVpp
Input Termination Impedance		Differential RXIN+ to RXIN-, DC		100		Ω
Input Return Loss		Differential, f<4GHz, device powered on		10		dB
Output Return Loss		Differential, f<4GHz, device powered on		10		dB
Low Frequency Cutoff		High pass 3dB point for RX system		15		kHz
Output Rise and Fall Times (20%-80%)		Slow, Rx_slew = '1'		120	160	ps
		Fast, Rx_slew = '0'		60	80	
Differential Output Swing		High swing mode[1] Low swing mode[1]	700 370		900 470	mVpp
Total Jitter, Tj		Measured over RX input voltage range			100	mUI pp
Output Resistance		RXOUT+/- Single ended to VDD_RXO	40	50	60	Ω
Rate select change time	t_ratesel	Using RATESEL pin			10	µs

1 Receiver differential output swing characterised at 155Mbps and 2^7-1 PRBS using DCA eye amplitude function

3.3.2. RSSI Indicator and Rx PD Regulator

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Voltage on RSSI pin		Ireg=2mA (10nF & 100Ω minimum load)	2.4			V
Current sourced by RSSI pin		Measured using Rx Power ADC	0		2000	µA

3.3.3. Receive Photocurrent LOS

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
RSSI LOS assert time					10	µs
RSSI LOS de-assert time					40	µs
Electrical Hysteresis		$20\log_{10}$ (RSSIdeassert / RSSIassert)	2		4	dB
RSSI LOS assert level range		Set by AVG_LOS_set, Address F4h	1.0		411	µA

3.3.4. OMA LOS

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
OMA LOS assert time	t_loss_on				100	µs
OMA LOS de-assert time	t_loss_off				20	µs
Electrical Hysteresis		$20\log_{10}$ (Vdeassert / Vassert)	2.5		5.5	dB
OMA LOS assert level		Set by OMA_LOS_set, Address F3h	10		50	mV

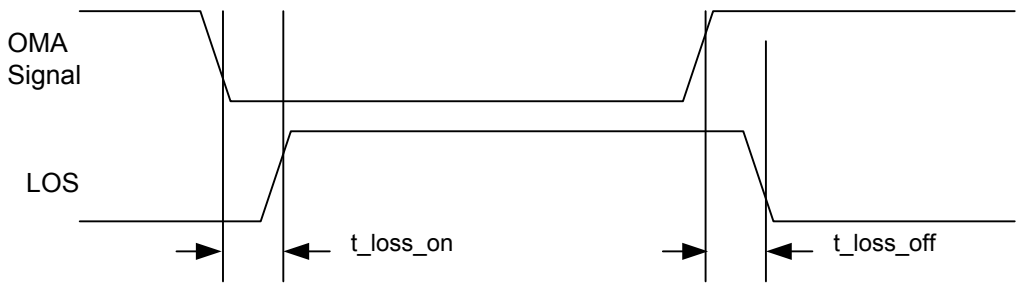


Figure 3 - OMA LOS Detection

3.4. Transmitter

3.4.1. Transmitter Inputs

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
High-Speed Data Input Signal Voltage[1]		Differential, AC-coupled, from 125Mbps to 2.125Gbps	200		1800	mVpp
High-Speed Data Input Impedance		Differential, DC	80	100	120	Ω
Input Return Loss		Differential, f<4GHz, device powered on		10		dB
Input common mode return loss		Both inputs shorted together, measured using 25Ω □source termination, 100MHz – 2.5GHz		10		dB

1 Differential inputs of up to 2400mV can be used without damage but performance specification is not guaranteed

3.4.2. VCSEL Driver

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Modulation Current	I_{mod}		0.5		16	mA
Electrical 20% to 80% rise / fall time		Measured using 50Ω□effective termination, AC and DC coupled applications		55	65	ps
Total Jitter contribution		Measured over modulation current range			100	mUI pp
VCSEL output compliance range		Allowed voltage for VCSEL driver output pins in dynamic operation, referenced to ground (VSS_TX).	600			mV
Bias current output compliance		Minimum allowed voltage for pin VCSEL_BIAS, referenced to ground (VSS_TX)	300			mV

3.4.3. VCSEL Mean Power Control Loop

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Bias Current			0.1		20	mA
Bias current off		Transmitter disabled			10	μA
Max current at MPD pin		Sink current			2.6	mA
Turn on/off overshoot		Bias current overshoot, Loop_BW=1			15	%
APC -3dB Loop Bandwidth	f_{Loop_BW}	Loop_BW = “0” Loop_BW = “1”		5 15		kHz
Bias loop settling time	t_settle	Loop_BW = “0” Loop_BW = “1”		5 500	10 1000	ms μs

3.4.4. Eye Safety Internal Fixed Limits

Operation outside these limits causes a TX_FAULT to be asserted

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Eye safety supply voltage range		Voltage on VDD_TXO or VDD_TX	2.7		3.9	V
RREF pin voltage limit		RREF voltage applied to pin after calibration	0.9		1.1	V

3.4.5. Fault Timing

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Time to initialize	t_init	From power on or application of Vcc>2.97V during plug in			300	ms
Hard TX_DISABLE assert time	t_off	Time from rising edge of TX_DISABLE to when the optical output falls below 10% of nominal			2	µs
Hard TX_DISABLE negate time	t_on	Time from falling edge of TX_DISABLE to when the modulated optical output rises above 90% of nominal			1	ms
Hard TX_Fault assert time	t_fault	Time from fault to TX_FAULT on			100	µs
TX_DISABLE pulse width	t_reset	Time TX_DISABLE must be held high to reset TX_FAULT	5			µs
TX_FAULT deassert time	t_faultdass	Time to deassert TX_FAULT after TX_DISABLE			300	ms

3.4.6. Diagnostic Timing Diagrams

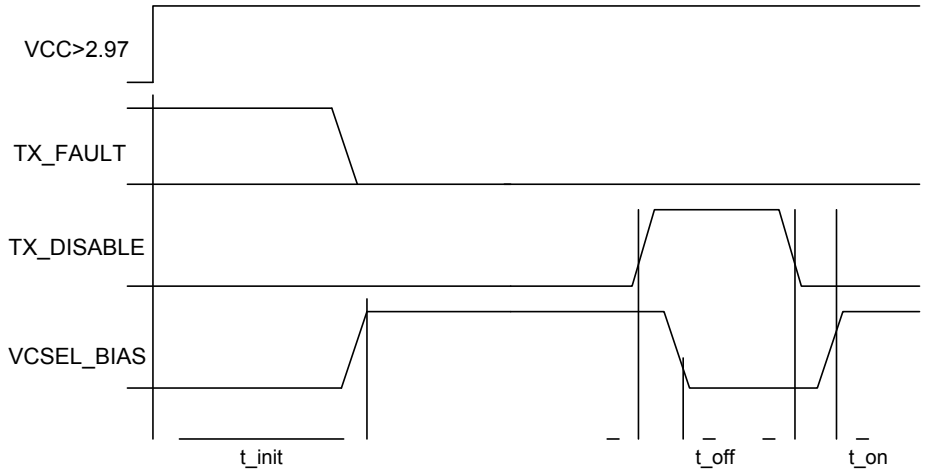


Figure 4 - Device turn on

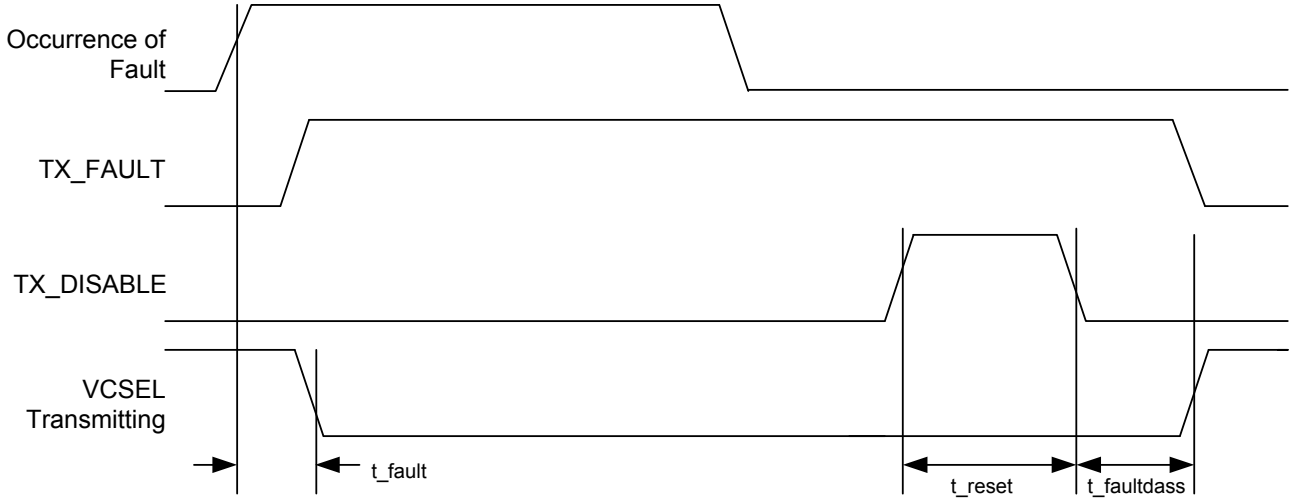


Figure 5 - Fault detection

3.5. 2-Wire Serial Interface

3.5.1. AC Electrical Characteristics

Parameter	Symbol	Comment	Min	Typ	Max	Unit
SCL clock frequency	f_{SCL}		0		100	kHz
LOW period of the SCL clock	t_{LOW}		4.7		–	µs
HIGH period of the SCL clock	t_{HIGH}		4.0		–	µs
Set-up time for a repeated START condition	$t_{SU:STA}$		4.7		–	µs
Hold time (repeated) START condition	$t_{HD:STA}$		4.0		–	µs
Data hold time	$t_{HD:DAT}$		0		3.45	µs
Data set-up time	$t_{SU:DAT}$		250		–	ns
Rise time of both SDA and SCL signals	t_R		–		1000	ns
Fall time of both SDA and SCL signals	t_F		–		300	ns
Set-up time for STOP condition	$t_{SU:STO}$		4.0		–	µs
Bus free time between a STOP and START condition	t_{BUF}		4.7		–	µs
Output fall time from VIHmin to VILmax	tof	10pF < Cb(1) < 400pF	0		250	ns
Capacitance for each I/O pin	Ci		–		10	pF

1 C_b = capacitance of a single bus line in pF.

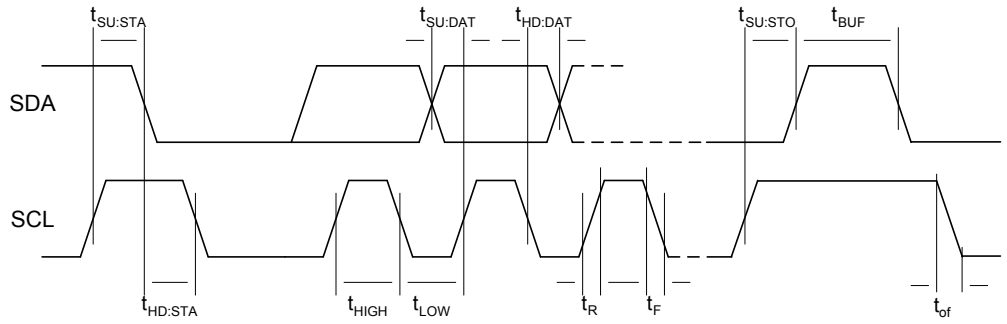


Figure 6 - SDA and SCL bus timing

3.5.2. DC Electrical Characteristics

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Low level input voltage	V_{IL}		- 0.5		0.3 VDD	V
High level input voltage	V_{IH}		0.7 VDD		VDD + 0.5	V
Low level O/P voltage	V_{OL}	3 mA sink current	0		0.4	V
I/P current each I/O pin	I_i	$0.1VDD < V_i < 0.9VDD$	-10		10	mA

3.6. DC Characteristics: TX_FAULT; TX_DISABLE; LOS.

Parameter		Comment	Min	Typ	Max	Unit
LVTTL Voltage Out High		External 4.7k to 10k pull-up	Host VCC - 0.5		Host VCC + 0.3	V
LVTTL Voltage Out Low		External 4.7k to 10k pull-up	0		0.5	V
LVTTL Voltage In High		Internal pull-up	2.0		VDD + 0.3	V
LVTTL Voltage In Low		Internal pull-up	0		0.8	V
R pull-up		Internal pull-up	6		10	kΩ

3.7. Typical Operating Characteristics

3.7.1. Electrical Receiver Eye Diagrams (3.3V; Ta = 25°C; PRBS 2^7-1)

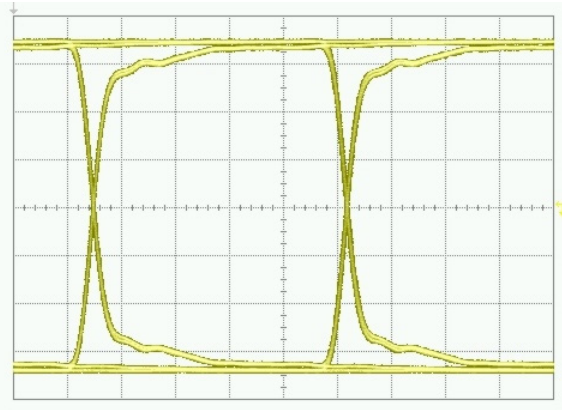


Figure 7 – 1.0625Gbps High swing mode

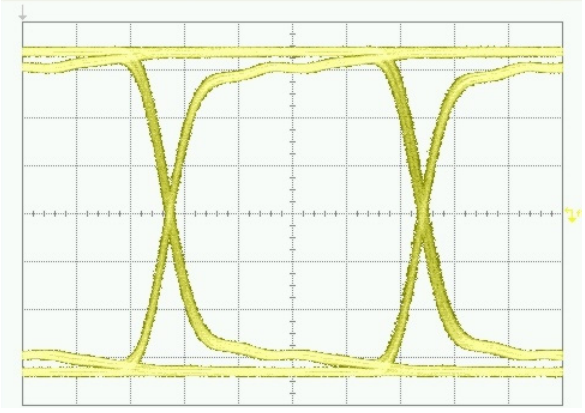


Figure 8 – 2.125Gbps Low swing mode

3.7.2. Optical Transmit Eye Diagrams (3.3V; Ta = 25°C; PRBS 2^7-1)

Transmitter setup with P_{mean} = -4.5dBm; E.R. =8.5dB; OMA=500µW

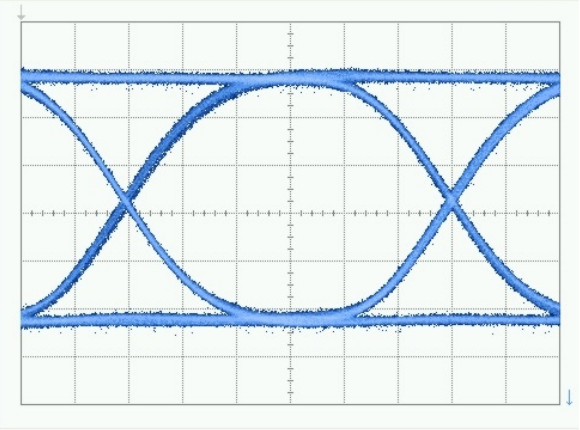


Fig 9 – 2.125Gbps; 60% margin

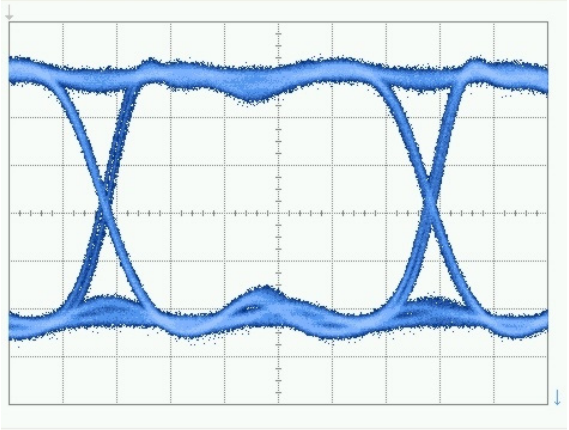


Fig 10 – 2.125Gbps; unfiltered rise and fall times 65ps

4. Functional Description

4.1. Overview

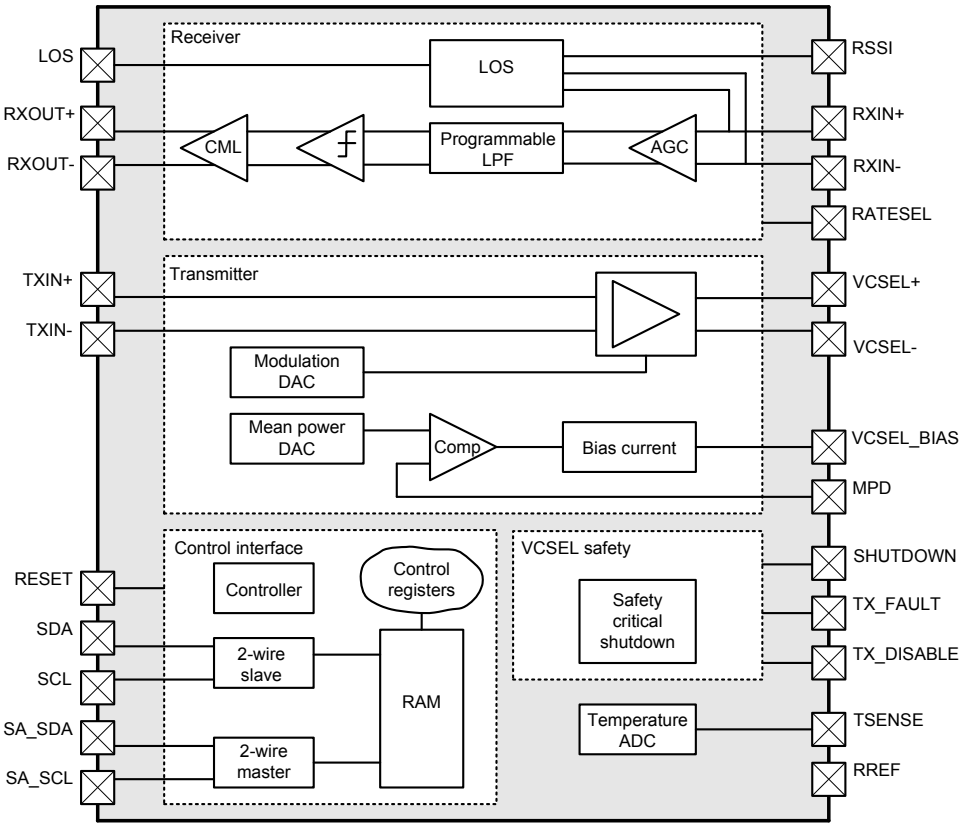


Figure 11 - Top-level block diagram of the PHY1071-01

4.2. Receiver Features

The receiver input is designed to be AC-coupled to the transimpedance amplifier, with internal 100Ω differential termination. The AGC amplifier is followed by a low-pass filter with programmable cut-off frequency, enabling the PHY1071-01 receiver to support five discrete data rates in the range 125/155 Mbps to 2.125 Gbps.

The filter output is followed by a limiting stage. For minimum duty cycle distortion, DC feedback from the limiter output is used for offset cancellation.

The output CML buffer completes the receiver chain, delivering the output at pins RXOUT+ and RXOUT-. The output edge rate is dependent on the programmable filter setting. Additionally, the output swing is programmable to satisfy different interface requirements (e.g. CML, ac-coupled LVPECL compatible).

The PHY1071-01 includes a regulator to deliver a controlled voltage to the receiver photodiode cathode at the RSSI pin. The current at RSSI is digitized for use in measuring the received signal strength. This signal can also be used to generate a Loss of Signal (LOS) alarm, with a pre-set hysteresis for assert and de-assert levels. The LOS assert threshold can be adjusted using the LOS LEVEL DAC.

Alternatively, the LOS alarm can be programmed to detect the amplitude of the AC signal, the Optical Modulation Amplitude (OMA) at the receiver input. The OMA LOS assert threshold can be adjusted using the RX AMP DAC.

4.2.1. Input Stage Configuration

The differential RXIN inputs from the ROSA can be terminated to a common mode voltage. This should be used for all recommended application frequencies of the PHY1071-01, where the inputs are AC coupled. The common mode voltage should be connected by setting **RX_dccouple** = '0' (E8h **rxControl0** bit 3).

4.2.2. Rate Selection

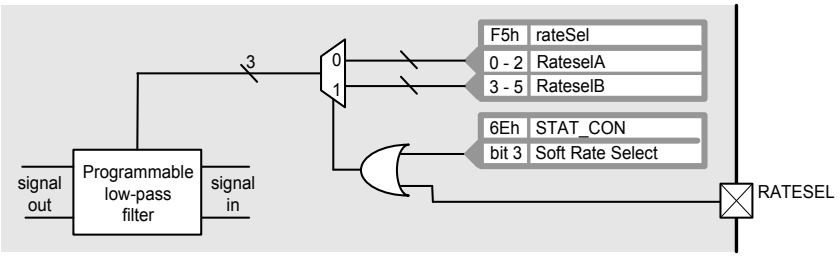


Figure 12 - Low pass filter rate selection

A programmable low pass filter provides band limiting in the received signal path. The filter bandwidth is set to 0.75 x signal data rate for optimum signal to noise performance and is controlled by a 3-bit control word as shown in Table 1.

The rate selection register, **rateSel**, stores two 3-bit codes for controlling the filter; code A in bits 0 to 2, and code B in bits 3 to 5. The selection between the two codes is determined by the RATESEL pin and the **Soft Rate Select** bit as shown in Figure 12. Thus, the RATESEL pin can be used to switch between two pre-selected rates.

The **rateSel** register is unique in that it is directly accessible from the 2-wire serial slave interface. Write accesses are routed to both the register in hardware and the RAM. Read accesses read the **rateSel** value from the hardware. This enables the PHY1071-01 to respond more quickly to updates of this register. This also means that during the initialisation sequence, the bandwidth of the receiver can be set up before the **dsfail** alarm is cleared (see section 5.2.2). This feature does not exist in the 2-wire serial master interface. When loading registers from EEPROM, **rateSel** is loaded via RAM in the same way as all other registers.

Bit			Data Rate
2	1	0	
0	0	0	125/155 Mbps
0	0	1	622 Mbps
0	1	0	1062 Mbps
0	1	1	1250 Mbps
1	0	0	2125 Mbps
1	0	1	N/A
1	1	0	N/A
1	1	1	N/A

Table 1 - Signal data rates supported by the low pass filter

4.2.3. CML Output Stage Configuration

The CML output stage has two slew rate settings. For maximum receiver eye opening set **CMLslew** = '0' (E8h **rxControl0** bit 0). To minimise emitted radiation set **CMLslew** = '1'. The slew rates are defined in the table of Parametric Performance characteristics for the Receive limiting amplifier (Section 3.3.1).

The signal swing can also be adjusted. Set **HiLoSwing** = '1' (E9h **rxControl1** bit 1) for higher amplitude differential output swing as defined in the table in section 3.3.1. Set **HiLoSwing** = '0' for lower amplitude output swing.

4.2.4. Loss Of Signal

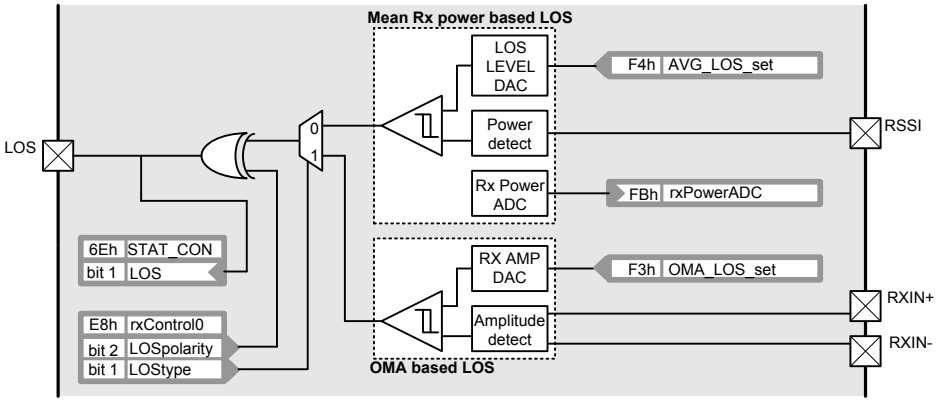


Figure 13 - Control of the LOS pin

Loss of signal (LOS) is determined in one of two ways. If **LOStype** = '1' then the optical modulation amplitude (OMA) method is selected. The signal amplitude measured at RXIN+/- is compared against a threshold level set by the **OMA_LOS_set** register. If the OMA does not exceed the threshold then the LOS pin and consequently the **LOS** bit in **STAT_CON** will be asserted.

If **LOStype** = '0' then the mean received power based method is selected. The signal power detected on the receiver signal strength indicator (RSSI) pin is compared against a threshold level set by **AVG_LOS_set**. If the RSSI does not exceed the threshold then the LOS pin and LOS bit are asserted.

The polarity of the LOS pin is controlled by **LOSpolarity**. If **LOSpolarity** = '0' then LOS is set high during a loss of signal condition. Conversely, if **LOSpolarity** = '1' then LOS is set high when a signal is detected.

Register	DAC	Step Size	Threshold Range
AVG_LOS_set	LOS LEVEL DAC (8 bits)	For Codes 00h – 1Fh Step Size = 1μA For Codes 1Fh – 7Eh Step Size = 4μA	0μA to 31μA 31μA to 411μA
OMA_LOS_set	RX AMP DAC (8 bits)	Use Codes 0Ah to C8 Step Size = 250μV (nominal DAC range = 0mV to 64mV)	10mV to 50mV

Table 2 - LOS DAC characteristics

For measurement of RSSI, which is used by SFF-8472 Digital Diagnostics Monitoring, the PHY1071-01 can be connected as shown in Figure 14, sourcing the photodiode bias current. This shows a PHY1093 TIA interfacing to the PHY1071-01. The photodiode used is biased using the regulated output of the PHY1071-01, providing a stable and low noise bias for the photodiode. The PHY1071-01 measures the photodiode current and generates a report of received signal strength via an on board A-D converter.

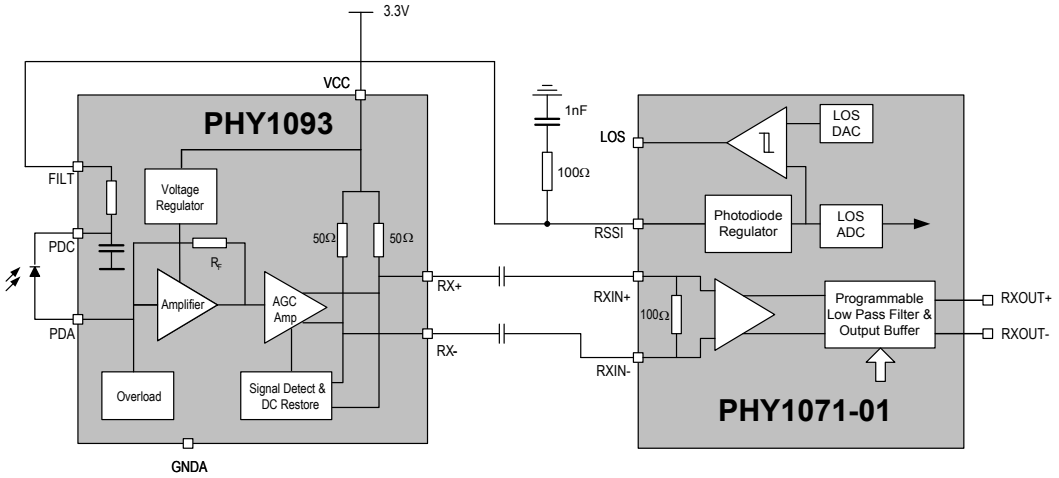


Figure 14: Connection to TIA for RSSI method of LOS detection

In some cases the TIA may source an output current which is proportional to the Received Signal Strength. In this case the application circuit shown in Figure 15 should be used. The current I_{RSSI} is mirrored using a dual NPN transistor as shown. This sinks an output current from the PHY1071-01 which can then be measured using the on chip DAC.

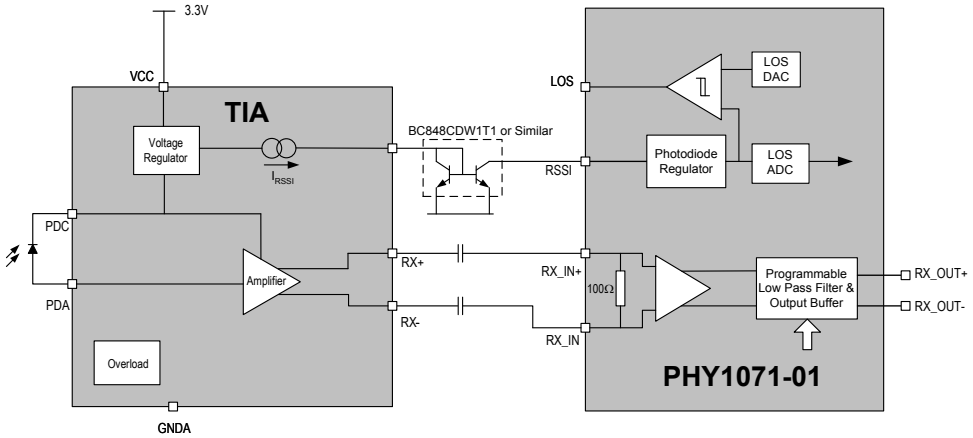


Figure 15: Connection to TIA with integrated RSSI output

4.3. Transmitter Features

The transmitter input buffer provides the necessary drive to the VCSEL driver output stage. It is designed to be AC-coupled, with an internal 100Ω differential termination.

The VCSEL driver output is designed to drive VCSELs in both common-cathode and common-anode configurations, using either AC or DC coupling. The driver circuit delivers a maximum peak to peak modulation current of 16mA. The maximum current delivered in DC-coupled mode is dependent on the VCSEL impedance. The voltage swing must remain in the compliance range of the output stage as specified in section 3.4.2.

The PHY1071-01 VCSEL driver operates with an analog mean-power control loop, which is digitally programmed using the Mean Power DAC. Modulation current is controlled by a VCSEL modulation DAC with the characteristics shown in Table 3. The modulation DAC has a 75µA/bit resolution which suggests an upper limit of 19.1mA at full scale, however the modulation output stage is rated to 16mA over operating temperature and voltage. To satisfy the digital diagnostics requirements, the mean power, as represented by the monitor photocurrent, is measured using the current monitor analogue to digital converter (Tx Power ADC). The bias current ADC (Tx Bias ADC) samples the VCSEL bias current.

Register	DAC	Step Size	Range
tx_power_set	Mean Power DAC (8 bits)	12µA (Actual DAC range 0µA to 3060µA)	0 to 3mA
modulationDACDefault	VCSEL modulation DAC[1] (8 bits)	75µA (Actual DAC range 0.5mA to 19.1mA)	0mA to 16mA

1 Range of modulation current measured at VCSEL+/- (jitter within spec)

Table 3 - Characteristics of the modulation and bias current DACs

4.3.1. Bias Current Control

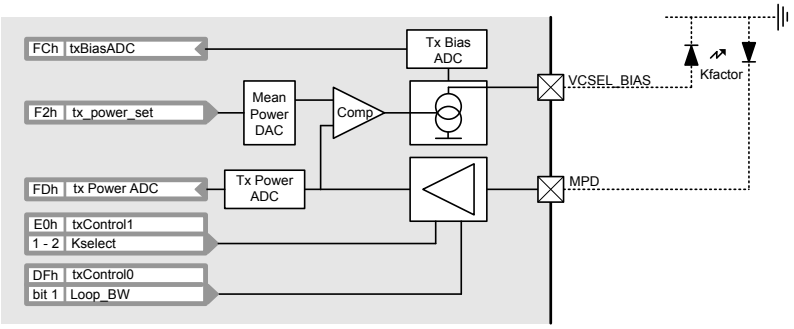


Figure 16 - Control registers affecting the APC loop

The VCSEL bias current is controlled by the mean-power control loop in which the current from the monitor photodiode in the TOSA is compared with a reference current controlled by **tx_power_set**. The mean-power control loop can be configured for either common-cathode or common anode VCSELs using the **MPC_polarity** bit of the **txControl0** (DFh) register.

Note: the comparator is sensitive to large step changes in the value written to **tx_power_set** (or a small step change at low values). This can cause the safety critical shutdown module to assert a TX_FAULT, as will writing zero to **tx_power_set**.

Loop gain is affected by the coupling coefficient (Kfactor) between the VCSEL and monitor photodiode. A configurable gain stage is included in the APC loop to compensate for this Kfactor. The **Kselect** bits control the gain stage and should be set up according to Table 4. For example, for a TOSA with Kfactor of 1/100 (VCSEL bias current = 15mA, monitor diode current = 0.15mA) set **Kselect** = “01”.

Kselect 1	Kselect 0	Coupling coefficient
0	0	1/500 – 1/150
0	1	1/150 – 1/50
1	0	1/50 – 1/25
1	1	1/25 – 1/8

Table 4 - Gain settings for the APC loop

The bandwidth of the control loop response can be controlled with **Loop_BW**. For a critically damped loop, set **Loop_BW** to '0'. For a more rapid response, set **Loop_BW** to '1'. The frequency response of the loop is detailed in section 3.4.3 VCSEL Mean Power Control Loop.

4.3.2. Modulation Current Control

The modulation current can be controlled in two ways:

Set **ModLUTdisab** (DFh **txControl0** bit5) to '1' to directly access the modulation DAC. Then, adjust modulation current by writing to **modulationDACDefault** (D5h).

Set **ModLUTdisab** to '0'to enable the modulation current vs. temperature look-up table (LUT) in the PHY1071-01. The 45 byte LUT is indexed by the value in **temperatureADC** (FEh), where Index is given by:

Index = (**temperatureADC** x 45) / 255

and the index rounds down to the lower temperature.

When the LUT is switched from the enabled to disabled state, the last control value from the LUT will persist. On disabling the LUT the modulation DAC will not revert back to a value previously written to **modulationDACDefault**. A new value must be explicitly written to **modulationDACDefault** once the LUT has been disabled.

On power up the modulation DAC will not be programmed with the value uploaded from the EEPROM and will default to taking the value from the LUT for the measured temperature.

4.3.3. VCSEL Driver Setup

There is a trimming network on the output driver which adjusts the time constant for output damping on VCSEL ± . It is controlled by the value in **txDriverCap** (F6h) which is used to select between 1 and 8 capacitors connected to the VCSEL± outputs as shown in figure 17. All capacitors are ~0.8pF. Set **txDriverCap** to '00h' for no damping and fastest edges; set to 'FFh' for full damping and slowest edges.

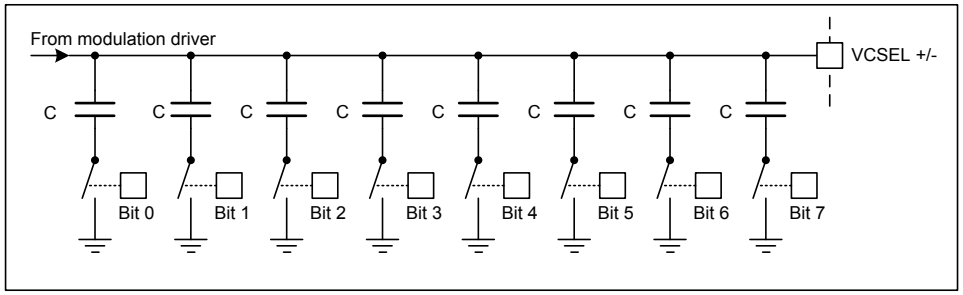


Figure 17 -Time constant selection for the Tx output damping network.

4.4. VCSEL Safety Features

The VCSEL safety circuitry monitors the device for potential faults. If a fault is detected, the safety logic turns off the transmitter bias and modulation currents and indicates the fault condition at pin TX_FAULT.

The VCSEL output driver can be disabled in one of four ways:

1. The TX_DISABLE pin is taken high.
2. The internal safety critical shutdown circuitry detects a fault with
    a. the APC loop or bias current
    b. power supply 2.7V>VDD or VDD>3.9V
    c. RREF shorted to Ground, VDD or open circuit
3. The **Soft Tx Disable** bit in **STAT_CON** is asserted
4. The watchdog timer times out, indicating that communication with the host/MCU has been interrupted.

In all cases the modulation current and the current to the VCSEL_BIAS pin will be disabled, and the SHUTDOWN pin will be asserted. The purpose of the SHUTDOWN pin is to provide a means by which the VCSEL can be isolated from ground (common cathode configuration) when an electrical fault is detected. In cases 2 and 4, TX_FAULT will also be set.

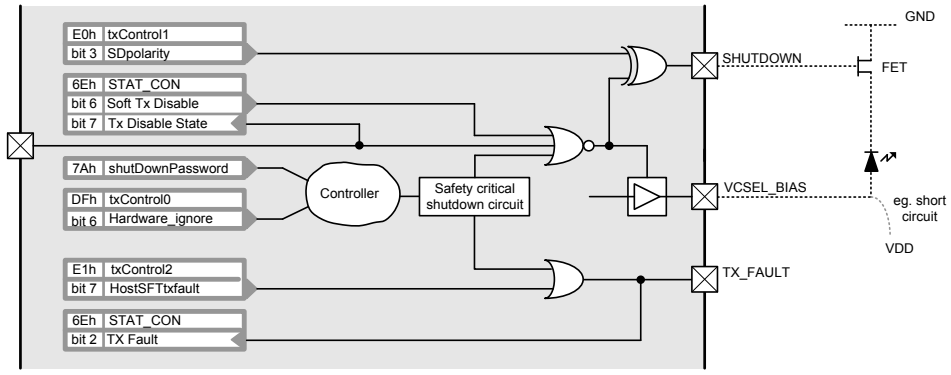


Figure 18 - TX_FAULT and SHUTDOWN pin control logic

4.4.1. PHY1071-01 Fault Management

The safety critical shutdown circuit will shutdown and isolate the VCSEL if it senses a fault with the bias current, the supply voltage or the reference voltage.

For example, consider a VCSEL arranged in common cathode configuration. The VCSEL anode connects to the VCSEL_BIAS pin and the cathode connects to ground. If a short circuit to VDD occurs on the route between the anode and VCSEL_BIAS then the safety critical shutdown circuit will switch off the bias current. However, this will not protect the laser as a current path from VDD to ground still exists. A FET device can provide the required isolation when switched off by the SHUTDOWN pin as shown in figure 18. The SHUTDOWN pin is controlled by the same signal which switches off the bias current. The SHUTDOWN pin output response to faults and polarity setting is shown in table 6.

In common anode configuration the polarity of the SHUTDOWN pin needs to be reversed. The polarity of the shutdown pin is controlled by **SDpolarity**.

The safety critical shutdown circuit can be disabled in software by setting **Hardware_ignore** = '1', and entering the value 42h to the **shutDownPassword** register. In this case the VCSEL will not be disabled when a fault is detected; however, a TX_FAULT will still be reported. **This feature should be used with great caution as the eye safety features of the device will be disabled.**

The PHY1071-01 will respond to TX_DISABLE being set even if **Hardware_ignore** is set.

Power supply and VREF faults result in the TX_FAULT latching and the laser being disabled momentarily. Once the fault condition is removed the laser will be reactivated, however the TX_FAULT output must be cleared by toggling TX_DISABLE (or **Soft Tx Disable**). An APC loop fault results in the TX_FAULT latching and the laser being disabled. TX_DISABLE (or **Soft Tx Disable**) must be pulsed high as shown in Figure 5 to remove this latching condition and reactivate the laser. When the Laser is turned on, during power up or after a fault, there will be a short period during which the bias control loop is allowed to settle (t_settle, see Section 3.4.3) before the safety control loop circuit is enabled.

Fault Status	SDpolarity (TxControl2, Bit 3)	SHUTDOWN Pin Voltage
No Fault	0	High
	1	Low
Fault	0	Low
	1	High

Table 5 – Shutdown Output Voltage under Fault/No Fault conditions

4.4.2. MCU and Host Fault Management

The MCU is responsible for maintaining and reporting alarms and warnings in accordance with the SFF-8472 specification. When an alarm is triggered, the MCU must set **HostSFTtxfault** = '1'. This will cause the PHY1071-01 to report a fault on the TX_FAULT pin and in the **STAT_CON** register. The PHY1071-01 will not disable the VCSEL at this point. The MCU or the host could disable the VCSEL when a **TX Fault** is detected in **STAT_CON** by asserting **Soft Tx Disable**.

4.4.3. Watchdog

A watchdog is implemented by the PHY1071-01 to monitor the activity of the attached MCU in digital diagnostics mode. When **WatchdogEn** (E1h **txControl2** bit0) is set to '1', the PHY1071-01's watchdog feature is enabled. The MCU is required to increment the **Watchdog[0:5]** counter (E1h **txControl2**) at least every 100ms. If no change is detected in the counter, the PHY1071-01 will disable the VCSEL and will assert TX_FAULT. The VCSEL will be re-enabled, and TX_FAULT de-asserted when either the watchdog counter is incremented, or the watchdog feature is disabled by writing '0' to **WatchdogEn**. On power up the watchdog feature is disabled.

4.5. Tsense Temperature Sensor

The temperature is determined by measuring the ΔV_{BE} across an external transistor connected to the TSENSE pin. The transistor can be any standard npn silicon transistor with a beta > 100 connected in diode mode (base and collector tied together). Phyworks recommends using a BC847 or similar.

Calibration and averaging of the temperature sensor readings using an external microcontroller are required to optimise the accuracy. Once optimised, the PHY1071-01 can report temperature to SFF8472 requirements over the recommended operating conditions.

The temperature sensor operating range and corresponding TSENSE input levels are shown in Table 6.

	Symbol	Unit	Minimum	Maximum
Temperature	t	°C	-70	+115
TSENSE differential input voltage	ΔV_{BE}	mV	50	100

Table 6 – Temperature sensor operating range

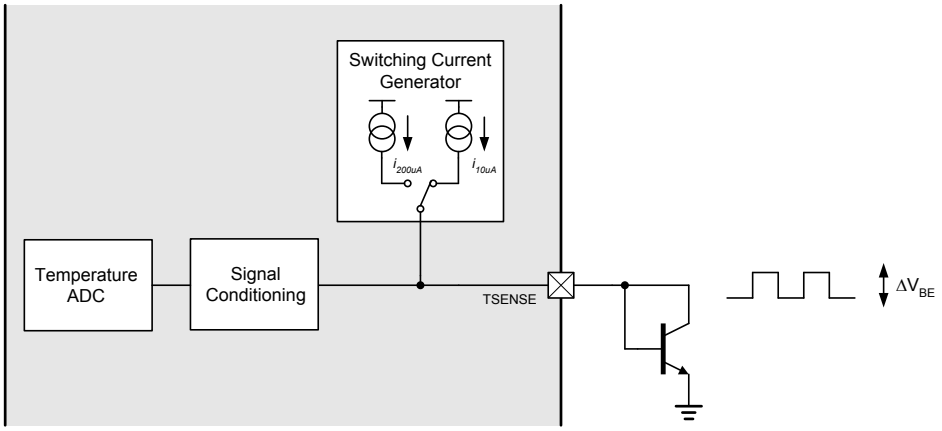


Figure 19 – Temperature sensor functional block diagram

5. Control Interface

The PHY1071-01 can be operated in one of two modes as dictated by the design of the module. The PHY1071-01 will identify the mode by attempting to read from its 2-Wire serial EEPROM interface (See section 5.4) on power up. If no EEPROM is present then diagnostic mode is inferred.

In digital diagnostics mode, the Micro Controller Unit (MCU) and EEPROM (Address A0h) present an SFF-8472 compliant interface to the host. The MCU provides read/write access to all registers in the A2h registers map, calculates digital diagnostics monitor values and maintains alarms and warnings. The MCU must initialise the PHY1071-01 control registers from EEPROM, relay control information to the PHY1071-01, and fetch status information in real time.

In Stand-alone mode, the PHY1071-01 is initialised directly from an external 4 kbit (8 x 512 bit) Serial EEPROM. Serial ID information as specified in the SFP MSA is accessible via the two wire interface. This mode supports temperature compensation of modulation current using a look-up table stored in EEPROM.

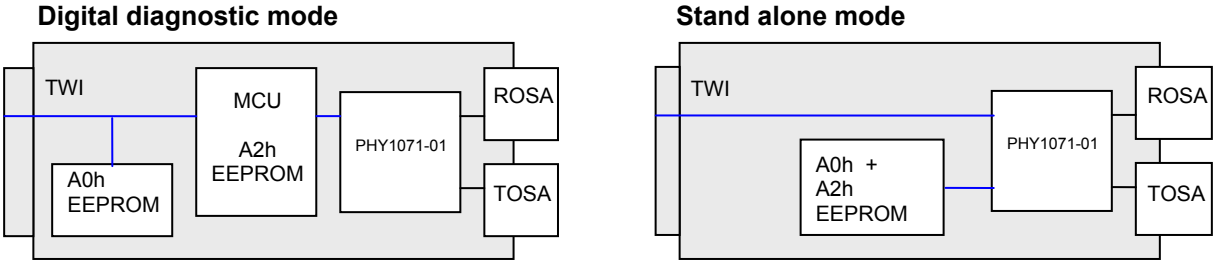


Figure 20 - Optical transceiver module configurations

5.1. Memory Map

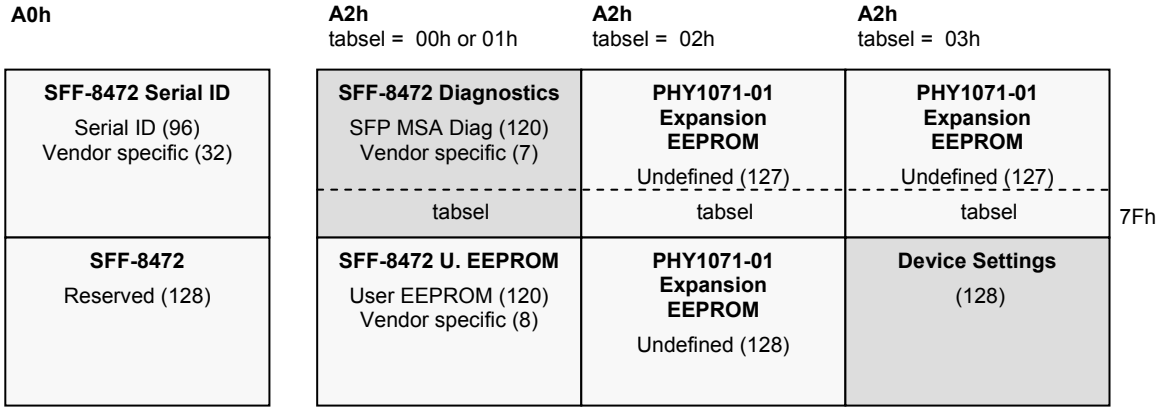


Figure 21 - Memory map for a 2G SFP or SFF transceiver module containing a PHY1071-01 device

Figure 21 shows the memory map of a module containing a PHY1071-01. An 8 kbit memory space is a natural step up from the minimum 4 kbit memory space required for SFF-8472 compliance, providing additional space in which to map the Device Settings registers of the PHY1071-01.

The internal RAM of the PHY1071-01 implements the SFF-8472 Diagnostics table and the Device Settings table. Selection between tables is achieved using the **tableSelect** (tabsel) register located at address offset 7Fh. To access the Diagnostics table, first write 00h to tabsel. To access the Device Settings table, first write 03h to tabsel.

Tabsel is effectively write-only because to write to tabsel has the effect of switching to a different register table. Thus, reading tabsel will not yield the value which was previously written.

5.2. Operation

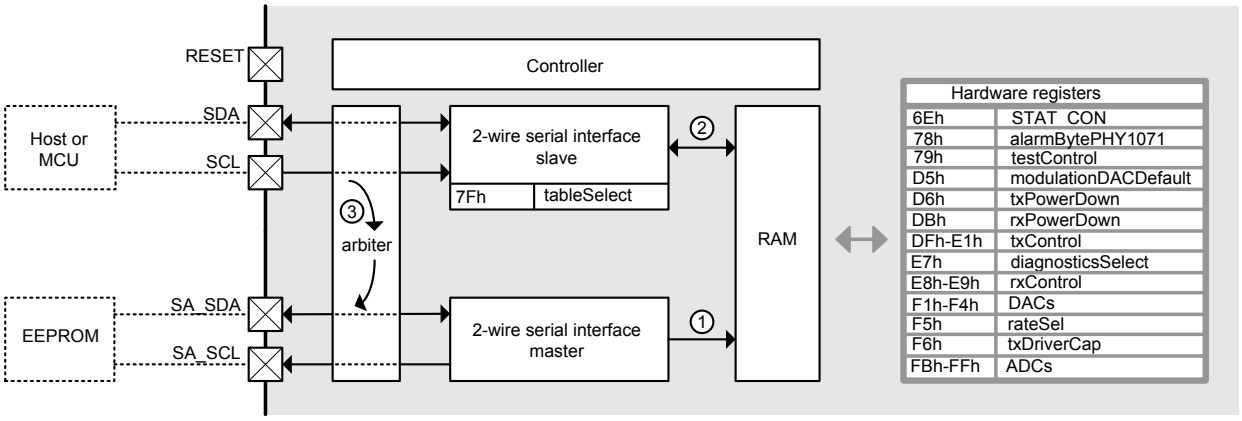


Figure 22 - Serial interfaces to RAM and the on-chip controller

5.2.1. Data Transfer Mechanisms

Three distinct data paths are identified in Figure 22.

When the PHY1071-01 comes out of reset, the 2-wire serial slave interface is disabled. Only path 1 is active. The controller instructs the 2-wire serial master interface to attempt to transfer A2h register tables (SFF-8472 diagnostics and device settings) from the external EEPROM to RAM. If this is successful then the PHY1071-01 will operate in stand-alone mode. If the transfer fails, then the **dsfail** and **eerxfail** alarm bits in the **alarmBytePHY1071** (78h) register will be set and the PHY1071-01 will operate in diagnostics mode. Regardless of the outcome, when the EEPROM read process is complete the controller enables the 2-wire serial slave interface. The 2-wire serial master interface is then no longer used.

The 2-wire serial slave interface has slave address A2h. In diagnostics mode, the host or external MCU uses the 2-wire serial slave interface to write to or read from copies of the device settings held in RAM. When the boot sequence is complete, the controller transfers data between the RAM and the actual registers implemented in hardware periodically every 10ms.

In stand-alone mode the RAM space is not used once the boot sequence is complete. Reading from A2h will return zero.

Path 3 is a special case which supports modules designed for stand-alone mode, enabling them to be set up or re-configured via the 2-wire serial interface slave. The PHY1071-01 can be forced into diagnostic mode if the data integrity numbers in the EEPROM are deliberately erased (see section 5.4.2). This enables the host/MCU to access both the RAM (path 2) and the EEPROM (path 3). All accesses to the A0h address space are directed to the EEPROM only. Accesses to the A2h address space are examined as they arrive by the 2-wire serial slave module, which in turn instructs the arbitration logic. The destination for the transaction depends on the value of tabsel and the register address as shown in Table 7.

Access type	tabsel	Address range[1]	Destination memory
read	00	lower	RAM
read	03	upper	RAM
write	00	lower	RAM + EEPROM
write	00	upper	EEPROM
write	03	upper	RAM

1 Addresses 00h to 7Fh = lower. Addresses 80h to FFh = upper.

Table 7 - Destination of 2-wire serial interface transactions as a function of tabsel and address.

5.2.2. Device Initialisation Sequence

The Initialisation Sequence is illustrated in Figure 23. The **Data_Ready_Bar** bit in the **STAT_CON** register indicates when data from the ADCs may be read after power up. It is first set to '1' before the 2-wire serial slave interface is enabled to indicate that the PHY1071-01 is not ready. Once initialisation is complete and the ADC data is ready **Data_Ready_Bar** is cleared to '0'. This event can be used by the external host/MCU as a signal that the PHY1071-01 is ready for device settings to be uploaded from the MCU to the PHY1071-01 RAM. The PHY1071-01 will not enter the main diagnostic function loop until the upload is complete. This is initiated by the host/MCU clearing the **dsfail** and **eerxfail** bits in the **alarmBytePHY1071** (78h) register. When **dsfail** is cleared and the main loop is executed the contents of RAM will be transferred into the hardware registers of the PHY1071-01.

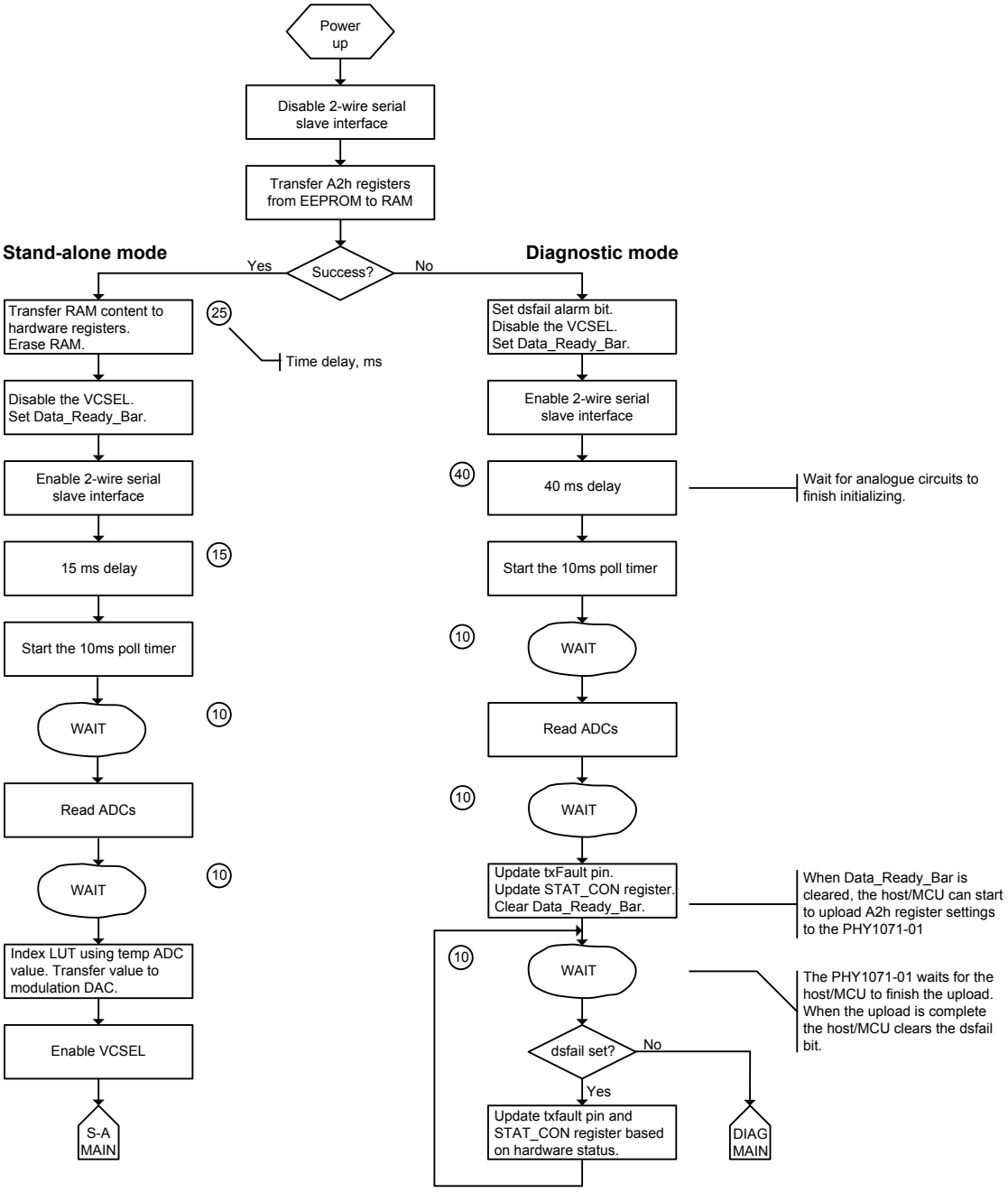


Figure 23 - PHY1071-01 initialisation sequence. Time delays for key stages are shown in ms.

5.2.3. Polling Loop Timer

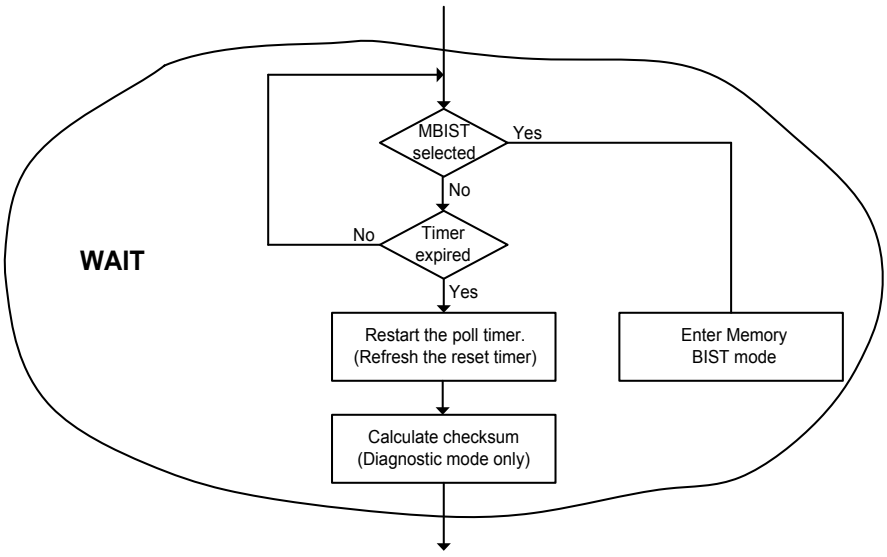


Figure 24 - PHY1071-01 polling loop timer function.

A polling loop timer is implemented in the controller which expires every 10ms. This is used to schedule functions in both the boot sequence and the main diagnostic and stand-alone operating modes. The WAIT clouds shown in the flow diagrams represent the sequence of events shown in Figure 24.

The reset timer is the timer enabled by **wdInhibit** in the **diagnosticsSelect** register (E7h). Refer to the registers map for details.

The checksum function is executed in diagnostic mode only. The PHY1071-01 will generate a checksum of the device settings RAM area by addition of each of the bytes listed in Table 8, and store the result in the 16 bit **ddmChecksum** register (E5h to E6h) in big endian format. The checksum will allow the MCU to efficiently verify that the copies of these registers in the PHY1071-01 and in its own memory are coherent.

Address	Size (bytes)	Name
80h	40	Reserved
A8h	45	currentLUT
D6h	1	txPowerDown
D7h	4	undefined
DBh	1	rxPowerDown
DCh	3	undefined
E8h	2	rxControl
F1h	1	Vref
F2h	1	tx_power_set
F3h	1	OMA_LOS_set
F4h	1	AVG_LOS_set
F5h	1	rateSel

Table 8 - Registers included in the checksum calculation

5.2.4. Controller Main Application Loop Functions

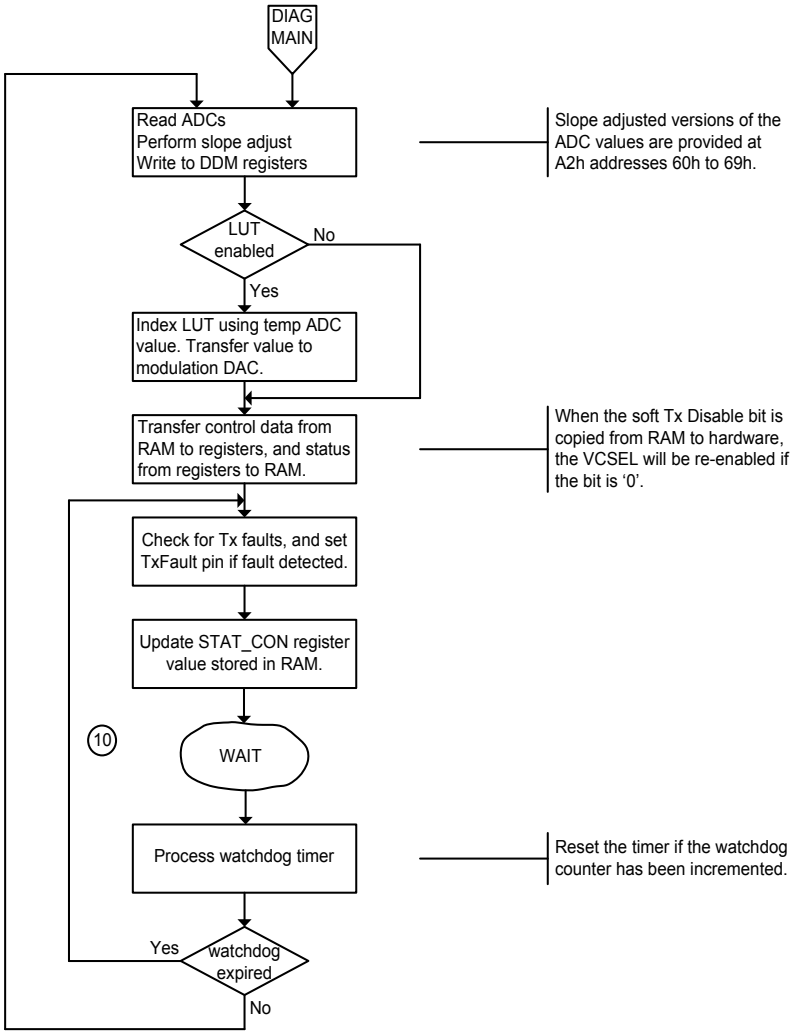


Figure 25 - PHY1071-01 diagnostic mode main loop function.

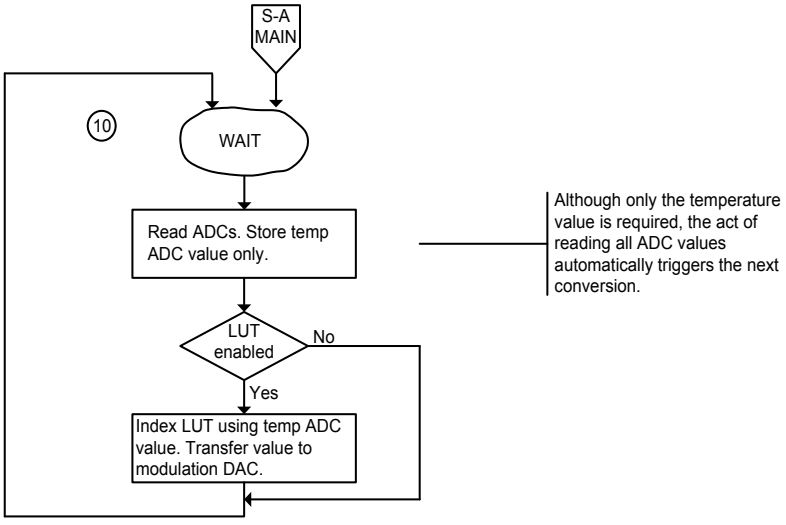


Figure 26 - PHY1071-01 stand-alone mode main loop function.

5.3. Digital Diagnostics Mode

5.3.1. Introduction

When used in digital diagnostic mode the PHY1071-01 contains all of the necessary analogue and digital circuitry to generate the real time values required for SFF-8472 DDM reporting compliance. The Power supply voltage, Temperature, TxBias, MPD and RSSI are all sampled using an on board A/D converter. The digitised values are then made available over the slave 2-wire serial interface, such that they can be used in conjunction with SFF-8472 calibration constants, to provide the host user with the following five real time reports: Supply Voltage, Temperature, Tx Bias current, Tx Output Power and Rx Input Power.

5.3.2. On Chip Analogue to Digital Converter

The PHY1071-01 contains a single successive approximation ADC, comprising an 8-bit DAC followed by a selectable gain stage. The gain stage is either linear or multi-slope, depending on the selected input from one of the five physical parameters being sampled. The multi-slope stage enables the ADC to cover the very large dynamic range required for reporting Tx and Rx optical power within the SFF-8472 limits, using only 8-bits to cover an equivalent 12-bit dynamic range. The ADC conversion time takes approximately 1ms.

5.3.3. ADC Characteristics

DDM Name	ADC input	Nominal Range	Step Size	Accuracy
Supply Voltage	VDD	1.7V to 4.4V	10.6 mV	± 3%
Temperature	Temperature	-70°C to +115°C	PHY1071-01 = 0.83 °C	± 3°C
Tx Bias	TxBias	0.0mA to 25.5mA	0.1mA	± 5%
Tx Power	MPD	0.0µA to 2448.0µA	1 µA : 0.0µA to 32.0µA	± 5%
			4µA: 32.0µA to 416.0µA	
			16uA: 416.0µA to 2448.0µA	
Rx Power	RSSI	0.0µA to 2448.0µA	1uA: 0.0µA to 32.0µA	± 5%
			4uA: 32.0µA to 416.0µA	
			16uA: 416.0µA to 2448.0µA	

Table 9 – ADC electrical characteristics

5.3.4. 3-Slope ADC

Tx and Rx Power DDM reports are represented by an 8 bit (0-255) ADC value even though the overall dynamic range for both of these parameters is 0µA to 2448 µA. A linear coding scheme would only provide 9.5µA resolution at low currents. Acceptable low current resolution coupled with wide dynamic range is possible by using a multi-slope gain stage within the ADC circuitry. The following formulae are used to convert the 8-bit ADC (0 to 255) value into a linear pseudo 12-bit ADC (0 to 2448) value:

$0 < ADC \leq 32$: $ADC\_L = ADC$

$32 \leq ADC \leq 128$ $ADC\_L = ((ADC - 32) * 4) + 32$

$128 \leq ADC \leq 255$ $ADC\_L = ((ADC - 128) * 16) + 416$

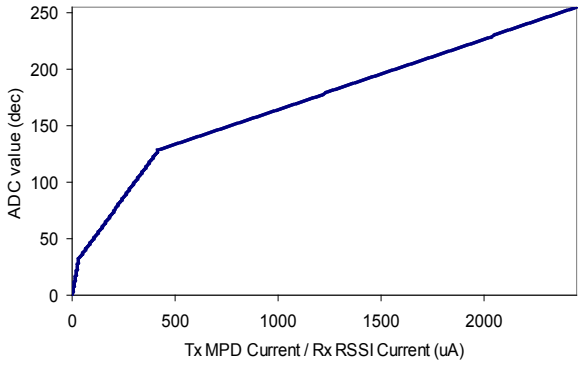


Figure 27 – 3-slope ADC Function

5.3.5. ADC DDM Register Locations

The 8-bit ADC values can be accessed in their raw format at addresses FBh to FFh (tabsel = 03h). The ADC values are also accessible at addresses 60h to 69h (tabsel = 00h) where Tx Power and Rx Power ADC values are linearised by the PHY1071-01 and, therefore, do not require any conversion from 3-slope format unlike the raw 8-bit ADC values.

An external MCU is required to apply the correct calibration *slope* and *offset* values to the PHY1071-01 ADC DDM reports in order that the real time reports are meaningful. Table 10 shows the memory locations that should be addressed on the 2-wire slave interface to access the various DDM ADC values. All 8 bit or 12 bit ADC values are left aligned into the 16 bit registers with unused bits set to zero. For example the MSBit of Tx Output Power is located at the MSBit of 66h (tabsel = 00h).

Address	Location	Name	Size
Table Select Byte (7F) = **00h**			
A2h	60h to 61h	Temperature	16-bit
A2h	62h to 63h	Vcc	16-bit
A2h	64h to 65h	Tx Bias	16-bit
A2h	66h to 67h	Tx Power	16-bit
A2h	68h to 69h	Rx Power	16-bit
Table Select Byte (7F) = **03h**			
A2h	FBh	rxPowerADC	8-bit
A2h	FCh	txBiasADC	8-bit
A2h	FDh	txPowerADC	8-bit
A2h	FEh	temperatureADC	8-bit
A2h	FFh	vddADC	8-bit

Table 10 – ADC DDM register locations

5.4. Stand-Alone Mode

In Stand-alone mode, the PHY1071-01 is initialised directly from an external 4 kbit (8 x 512 bit) Serial EEPROM. Serial ID information as specified in the SFP MSA is accessible via the 2-wire serial interface. This mode supports temperature compensation of modulation current using a look-up table stored in EEPROM.

5.4.1. Data Integrity Checking

The (read-only) ADCs located at addresses FBh to FFh are dual-functioned with (write-only) data integrity registers as follows:

Addr	Register	Value(hex)
FBh	SerialEepromIdentifier0	1Bh
FCh	SerialEepromIdentifier1	2Ch
FDh	SerialEepromIdentifier2	3Dh or 4Eh
FEh	SerialEepromChecksum0	--
FFh	SerialEepromChecksum1	--

Table 11 - Mapping of the data integrity numbers

On power-up, the PHY1071-01 will attempt to load its RAM from the EEPROM. If this is unsuccessful then **eerxfail** and **dsfail** are both set to '1' (78h **alarmBytePHY1071**) and initialisation will be stalled. If the transfer is successful then the integrity of the data will be checked.

The PHY1071-01 checks that the data read from EEPROM at addresses FBh to FDh matches the values shown in Table 11. If there is a mismatch then **dsfail** is set to '1' and initialisation will be stalled.

If **SerialEepromIdentifier2** = 3D then the PHY1071-01 will accumulate a 16 bit checksum for the A2h RAM address range 00h to FAh (excluding 7Fh). If this accumulated checksum does not compare correctly with the two **SerialEepromChecksum** bytes, then **dsfail** will be set to '1' and initialisation will be stalled.

Once all checks are complete, if no alarms have been set then the hardware registers in the PHY1071-01 are updated from the RAM. Data in RAM addresses FBh to FFh will subsequently be overwritten by the ADCs.

5.4.2. Device Setup

If a module is powered up with a blank or corrupted EEPROM then the data integrity checking will fail and initialisation is stalled. However, the PHY1071-01 can be forced into a 'setup' mode if the **dsfail** alarm is cleared by the host. This then permits the device to be configured and the EEPROM written in-system.

To reconfigure or analyse a module with its EEPROM already written, writing zero to the data integrity register addresses in EEPROM will have the effect of forcing the PHY1071-01 into setup mode the next time it is powered up.

5.4.3. Writing to EEPROM

The addressing of the RAM in the PHY1071-01 is consistent with the memory map for the module as a whole (see Figure 21). The table containing the SFF-8472 Diagnostics registers is selected by tabsel = 0 and the table containing the Device settings registers is selected by tabsel = 3.

The serial EEPROM connected to a PHY1071-01 in stand alone mode is typically small and is organised as shown below:

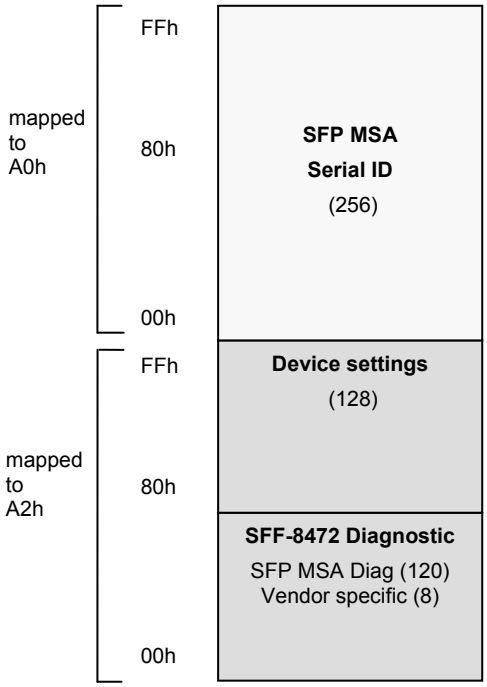


Figure 28 - Physical mapping of register tables into the EEPROM in the stand-alone mode

The device settings area in EEPROM is effectively stored in the address range normally occupied by the SFF-8472 User EEPROM (in Diagnostics mode). When writing to Device settings two separate write transactions are required: one write (into RAM) with tabsel = 3, and one write (into EEPROM) with tabsel = 0.

Phyworks recommends that the write protect functionality of the EEPROM is utilised to effectively protect stored settings after programming.

5.5. 2-wire Serial Interface

The PHY1071-01 has a pair of 2-wire serial interfaces - a slave for interfacing to an external MCU for use in diagnostics mode and a master for interfacing to an external EEPROM for use in stand-alone mode. Both interfaces communicate using the protocol described in this section.

5.5.1. Framing and Data Transfer

The two-wire interface comprises a clock line (SCL) and a data line (SDA). When the bus is idle both are pulled high within the PHY1071-01 by 8 kΩ pull-ups.

An individual transaction is framed by a start condition and a stop condition. A start condition occurs when a bus master pulls SDA low while the clock is high. A stop condition occurs when the bus master allows SDA to transition low-to-high when the clock is high. Within the frame, the master has exclusive control of the bus. The PHY1071-01 does not support REPEAT START conditions whereby the master may simultaneously end one frame and start another without releasing the bus by replacing the STOP condition with a START condition.

Within a frame, the state of SDA may only change when SCL is low. A data bit is transferred on a low-to-high transition of SCL. Data is arranged in packets of 9 bits. The first 8 bits represent data to be transferred (most significant bit first). The last bit is an acknowledge bit. The recipient of the data holds SDA low during the ninth clock cycle of a data packet to acknowledge (ACK) the byte. Leaving SDA to float high on the ninth bit signals a not-acknowledged (NACK) condition. The interpretation of the acknowledge bit by the sender will depend on the type of transaction and the nature of the byte being received.

5.5.2. Device Addressing

The first byte to be sent after a START condition is an address byte. The first seven bits of the byte contain the target slave address (msb first). The eighth bit indicates the transaction type – ‘0’ = write, ‘1’ = read. Each slave interface on the bus is assigned a 7-bit slave address. If no slave matches the address broadcast by the master then SDA will be left to float high during the acknowledge bit and the master receives a NACK. The master must then assert a STOP condition. If a slave identifies the address then it acknowledges the master and proceeds with the transaction identified by the type bit.

The slave interface of the PHY1071-01 can decode slave addresses A0h and A2h.

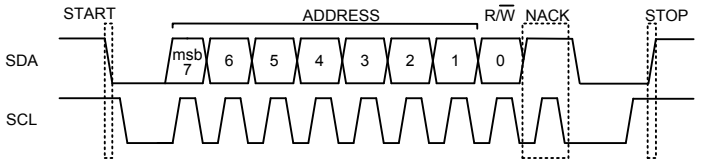


Figure 29 - Address decoding example – slave not available

5.5.3. Write Transaction

Figure 30 shows an example of a write transaction. The address byte is successfully acknowledged by the slave, and the type bit is set low to signify a write transaction. After the acknowledge the master sends a single data byte. All signalling is controlled by the master except for the SDA line during the acknowledge bits. During the acknowledge the direction of the SDA line is reversed and the slave pulls SDA low to return a ‘0’ (ACK) to the master.

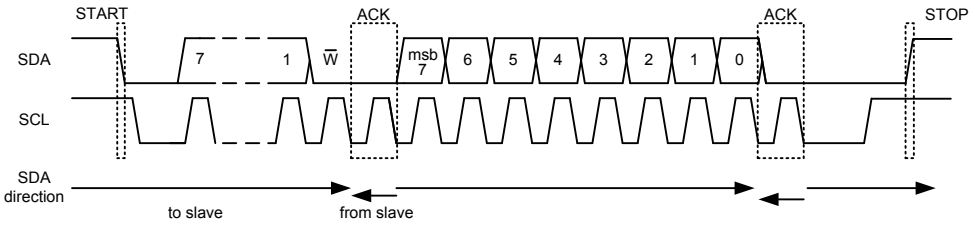


Figure 30 - Write transaction

If the slave is unable to receive data then it should return a NACK after the data byte. This will cause the master to issue a STOP and thus terminate the transaction.

The PHY1071-01 interprets the first data byte as a register address. This will be used to set an internal memory pointer. Subsequent data bytes within the same transaction will then be written to the memory location addressed by the pointer. The pointer is auto-incremented after each byte. There is no limit to the number of bytes which may be written in a single burst to the 256 byte internal RAM of the PHY1071-01.

If the slave is not ready to receive a byte then it may hold SCL low immediately after the acknowledge bit. When SCL is released the master starts to send the next byte. This is known as clock stretching. The PHY1071-01 slave interface will not clock stretch at up to100 kHz SCL frequency.

5.5.4. Read Transaction

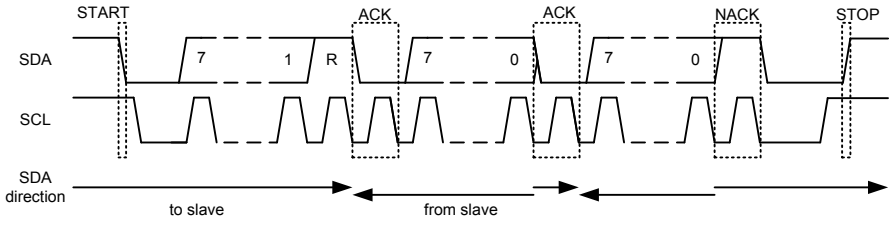


Figure 31 - Read transaction

Figure 31 shows an example of a 2 byte read transaction. The address byte is successfully acknowledged by the slave, and the type bit is set high to signify a read. After the ACK the slave returns a byte from the location identified by the internal memory pointer. This pointer is then auto-incremented. The slave then releases SDA so that the master can ACK the byte. If the slave receives an ACK then it will send another byte. The master identifies the last byte by sending a NACK to the slave. The master then issues a STOP to terminate the transaction.

Thus, to implement a random access read transaction, a write must first be issued by the master containing a slave address byte and a single data byte (the register address) as shown in Figure 30. This sets up the memory pointer. A read is then sent to retrieve data from this address (see Figure 31).

6. Register Map

All Phyworks specific registers are listed in this section. For details of other registers refer to the SFF-8472 Specification for Diagnostic Monitoring Interface for Optical Transceivers.

Where a single power-on reset (PoR) value is shown for a range of addresses, that value applies to all bytes in the range. Note that the power on reset values may be overwritten during initialisation by the MCU (or from EEPROM in stand-alone mode).

For registers containing a single 8-bit field, the most significant bit of the field is stored in bit 7 of the register byte. Multi-byte registers are stored in big-endian order unless specified otherwise.

Note that 'reserved' or 'internal use only' register bits are specified as read only. These registers should not change from their PoR default settings.

6Eh	**STAT_CON**			**Status and Control register for some SFF-8472 functions**
Bit	**Field name**	**Type**	**PoR**	
7	**Tx Disable State**	**R**	**0**	**Digital state of the TX Disable input pin. Updated within 100msec of change of pin.**
6	**Soft TX Disable**	**R/W**	**0**	**Read/write bit that allows software disable of laser. Writing '1' disables laser. This bit is "OR'd" with the hard TX_DISABLE pin value.**
5	**Reserved**	**R**	**0**	**Reserved for future use.**
4	**Rx Rate Select State**	**R**	**0**	**Digital state of the SFP RX Rate Select input pin. Updated within 100msec of change on pin.**
3	**Soft RX Rate Select**	**R/W**	**0**	**Soft RX Rate Select read/write bit that allows software RX rate select. Writing '1' selects full bandwidth operation. This bit is "OR'd" with the RATE_SELECT pin value.**
2	**TX Fault**	**R**	**0**	**Digital state of the TX_FAULT output pin. Updated within 100msec of change on the pin.**
1	**LOS**	**R/W**	**0**	**Digital state of the LOS output pin. Updated within 100msec of change on the pin.**
0	**Data_Ready_Bar**	**R**	**0**	**Indicates PHY1071-01 has achieved power up and data is ready. Bit remains high until data is ready to be read at which time the device sets the bit low.**

78h	alarmBytePHY1071			Status register for the PHY1071-01 control module.
Bit	Field name	Type	PoR	
7	Wd4	R	0	This counter records the number of times that the PHY1071-01 has reset itself due to an internal timeout. The timer is controlled by wdInhibit in the diagnosticsSelect register.
6	Wd3	R	0	
5	Wd2	R	0	
4	Wd1	R	0	
3	Wd0	R	0	
2	membistPassed	R	0	Built-in self test (BIST) result (‘1’ = passed) from memory test initiated by testControl register bit 1.
1	dsfail	R/W	0	Data structure corrupt (‘1’ = data integrity bytes read from EEPROM during power up are incorrect). Clearing this bit during initialisation is necessary in order to allow the PHY1071-01 to resume its normal mission mode functions.
0	eerxfail	R	0	Eeprom dma load fail (‘1’ = no response from EEPROM during power up)

79h	testControl			This register puts the device into various test modes and should not be written to during normal operation. It should always have value ‘0’.
Bit	Field name	Type	PoR	
7	ATBcontrol5	R/W	0	Analog Test Bus Control Bit0
6	ATBcontrol4	R/W	0	Analog Test Bus Control Bit1
5	ATBcontrol3	R/W	0	Analog Test Bus Control Bit2
4	ATBcontrol2	R/W	0	Analog Test Bus Control Bit3
3	ATBcontrol1	R/W	0	Analog Test Bus Control Bit4
2	ATBcontrol0	R/W	0	Analog Test Bus Control Bit5
1	startMemoryBist	R/W	0	Set to ‘1’ to initiate Memory built-in self test (MBIST)
0	scanTestMode	R/W	0	Set to 1’ to enter Scan test mode.

7Ah	shutDownPassword			Set to 42h to prevent the safety critical shutdown logic from disabling the VCSEL when a hardware fault is detected (see also txControl0).
Type	R/W	PoR	00h	

7Bh - 7Eh	reserved			--
Type	R	PoR	00h	

7Fh	tableSelect			Indirect addressing for register tables. 00h selects the SFF-8472 Diagnostics and user EEPROM register tables. 03h selects the PHY1071-01 Device settings table. Note that data read from this register is not valid.
Type	R/W	PoR	00h	

80h – A7h	reserved			--
Type	R	PoR	00h	

A8h– D4h	currentLUT			Modulation current vs. temperature Look-up table (LUT). The 45 entry LUT is indexed using the temperatureADC as follows: (temperatureADC x 45) / 255.
Type	R/W	PoR	00h	

D5h	modulationDACDefault			Controls the modulation current (DAC) when the LUT is disabled. During power up, the temperature is sampled and the DAC is re-loaded with a value from the LUT.
Type	R/W	PoR	00h	

D6h	txPowerDown			Selectively turns off the power supply to circuits in the transmitter module. '0' = power on. '1' = power off.
Bit	Field name	Type	PoR	
7	VDDmeaspwrd	R/W	0	-
6	TERMpwrd	R/W	0	-
5	DACpwrd	R/W	0	Power down DAC
4	DRIVERpwrd	R/W	0	Power down VCSEL driver
3	TXBIASpwrd	R/W	0	Power down transmit bandgap bias + current gen. (This will completely disable the IC).
2	DBuffApwrd	R/W	0	Power down data buffer
1	TEMPpwrd	R/W	0	Power down temperature sensor
0	SAFETYpwrd	R/W	0	Power down SAFETY logic

D7h-DAh	undefined			--
Type	R	PoR	00h	

DBh	rxPowerDown			Selectively turns off the power supply to circuits in the receiver module. '0' = power on. '1' = power off.
Bit	Field name	Type	PoR	
7	LIMITpwrd	R/W	0	Power down limiter
6	FILTpwrd	R/W	0	Power down RX filter
5	COMPSpwrd	R/W	0	ADC Comparator powerdown
4	AMPDETpwrd	R/W	0	Power down amplitude detector
3	REGpwrd	R/W	0	Power down regulator
2	AGCpwrd	R/W	0	Power down AGC amp
1	CMLpwrd	R/W	0	Power down CML (RX related)
0	RXBIASpwrd	R/W	0	Power down receiver bandgap bias + current gen.

DCh-DEh	undefined			--
Type	R	PoR	00h	

DFh	txControl0			Control bits for the transmitter circuits.
Bit	Field name	Type	PoR	
7	Osc_Mon	R/W	0	Multiplexes the internal oscillator onto TX_FAULT pin for monitoring (oscillator = '1', normal operation = '0')
6	Hardware_ignore	R/W	0	Soft Disable for Safety Critical Shutdown. Set to '1' to prevent VCSEL shutdown when the SCS circuits detect an electrical fault and asserts a tx fault condition.
5	ModLUTdisab	R/W	0	Modulation Current LUT loop control (disable LUT = '1')
4	SFTtxfault	R/W	0	(Internal use only. Set to '0'.)
3	DAC_ready	R/W	0	(Internal use only. Set to '0'.)
2	testBW	R/W	0	(Internal use only. Set to '0'.)
1	Loop_BW	R/W	0	Controls the average power control loop response. Set to '0' for critical damping.
0	MPC_polarity	R/W	1	This must match the configuration of the TOSA. For common anode connection, set to '1'. Common cathode = '0'.

E0h	txControl1			Control bits for the transmitter circuits.
Bit	Field name	Type	PoR	
7	Test_comp_hiZ	R	0	(Internal use only. Set to '0'.)
6	Test_compout_en	R	0	(Internal use only. Set to '0'.)
5	Test_compout	R	0	(Internal use only. Set to '0'.)
4	Test_koff	R	0	(Internal use only. Set to '0'.)
3	SDpolarity	R/W	1	Controls the polarity of the SD pin. (For SD pin = 0 for shutdown, set SDpolarity = 1).
2	Kselect1	R/W	0	Kselect[1:0] selects one of four gain settings for a gain stage in the automatic power control loop (see Table 4). This optimises the loop gain for the coupling coefficient of the TOSA.
1	Kselect0	R/W	0	
0	Tempsel3i	R	0	(Internal use only. Set to '0'.)

E1h	txControl2			Control bits for the transmitter circuits.
Bit	Field name	Type	PoR	
7	HostSFTtxfault	R/W	0	Set to '1' to assert a tx fault condition on the TX_FAULT pin.
6	Watchdog5	R/W	0	When the watchdog counter is enabled, it must be incremented at least once every 100ms. If this does not occur then the PHY1071-01 will disable the VCSEL and assert a tx fault condition. Incrementing the counter or disabling the watchdog will cause normal operation to resume.
5	Watchdog4	R/W	0	
4	Watchdog3	R/W	0	
3	Watchdog2	R/W	0	
2	Watchdog1	R/W	0	
1	Watchdog0	R/W	0	
0	WatchdogEn	R/W	0	Watchdog Function Enable (enable = 1)

E2h - E4h	txControlSpare			reserved
Type	R	PoR	00h	

E5h– E6h	ddmChecksum			16-bit checksum updated by the PHY1071-01 every 10ms. See section 5.2.3 for a detailed description.
Type	R	PoR	00h	

E7h	diagnosticsSelect			Diagnostic functions (for internal use) are controlled by this register.
Bit	Field name	Type	PoR	
7	-		0	spare
6	-	R	0	spare
5	-	R	0	spare
4	-	R	0	spare
3	-	R	0	spare
2	-	R	0	spare
1	wdInhibit	R/W	0	See also register 78h alarmBytePHY1071. Set to '1' to disable the timer and prevent the chip from resetting itself if the timer is not serviced. Set to '0' for normal operation.
0	tstclksel	R/W	0	Set to '1' to select the SA_SDA pin as the clock source for the digital macro instead of the internal oscillator.

E8h	rxControl0			Control bits for the receiver circuits.
Bit	Field name	Type	PoR	
7	AMPDET _dcfbdisable	R	0	(Internal use only. Set to '0'.)
6	Gc_disable	R	0	(Internal use only. Set to '0'.)
5	AGCdcfb_disable	R	0	(Internal use only. Set to '0'.)
4	Trimsel	R/W	0	(Internal use only. Set to '0'.)
3	RX_dccouple	R/W	0	For AC coupled input, set to '0' to terminate the differential signal at RXIN+/- to a common mode voltage. Set to '1' when the inputs are DC coupled.
2	LOSpolarity	R/W	0	LOS pin sense ('1'=Signal Detect;'0'=Loss of signal)
1	LOStype	R/W	0	LOS Detection Type ('1'=OMA;'0'=Mean RX power)
0	CMLslew	R/W	0	RXOUT+/- slew rate control. Set to '0' for a fast slew rate. Set to '1' for slow slew rate.

E9h	rxControl1			Control bits for the receiver circuits.
Bit	Field name	Type	PoR	
7	-	R	0	Spare
6	-	R	0	Spare
5	-	R	0	Spare
4	LorV	R	0	(Internal use only. Set to '0'.)
3	Fosctrim1	R	0	(Internal use only. Set to '0'.)
2	Fosctrim0	R	0	(Internal use only. Set to '0'.)
1	HiLoSwing	R/W	0	Controls the differential swing of the signal output on RXOUT+/- ('1' = high amplitude, '0' = low amplitude)
0	LIM_dcfbdisable	R	0	(Internal use only. Set to '0'.)

EAh - EFh	rxControlSpare			reserved
Type	R	PoR	00h	

F0h	undefined			--
Type	R	PoR	00h	

F1h	Vref			Reference voltage trim DAC. The reference voltage can be set by adjusting Vref until the desired voltage is seen at pin RREF. RREF is pulled to ground by a 10 KΩ resistor for a 1V reference.
Type	R/W	PoR	71h	

F2h	tx_power_set			Sets the Tx mean power loop reference monitor current DAC. This DAC therefore controls the average output power of the VCSEL.
Type	R/W	PoR	00h	

F3h	OMA_LOS_set			Sets the threshold level for optical measurement amplitude based LOS detection.
Type	R/W	PoR	00h	

F4h	AVG_LOS_set			Sets the threshold level for receiver signal strength indicator (RSSI) based LOS detection.
Type	R/W	PoR	00h	

F5h	rateSel			Controls the bandwidth of the programmable low pass filter in the receiver. The two rate selection fields A and B enable switching between two different bandwidths using the RATESEL pin.
Bit	Field name	Type	PoR	
7	OSC1	R/W	0	(Internal use only. Set to '0'.)
6	OSC0	R/W	0	(Internal use only. Set to '0'.)
5	RateselB2	R/W	0	Rate Selection B. Selects one of five cut-off frequency settings (see Table 1).
4	RateselB1	R/W	0	
3	RateselB0	R/W	0	
2	RateselA2	R/W	0	Rate Selection A. Selects one of five cut-off frequency settings (see Table 1).
1	RateselA1	R/W	0	
0	RateselA0	R/W	0	

F6h	txDriverCap			Selects between different time constants for the trimming network which controls the tx driver output damping (see figure 17).
Type	R/W	PoR	00h	

F7h-FAh	reserved			--
Type	R	PoR	00h	

FBh	rxPowerADC			This register is dual functioned. Reads received optical power, Rx ADC value. Writes data integrity value SerialEepromIdentifier0.
Type	R/W	PoR	00h	

FCh	txBiasADC			This register is dual functioned. Reads VCSEL bias, Tx Bias ADC value. Writes data integrity value SerialEepromIdentifier1.
Type	R/W	PoR	00h	

FDh	txPowerADC			This register is dual functioned. Reads transmit optical power, Tx Power ADC value. Writes data integrity value SerialEepromIdentifier2.
Type	R/W	PoR	00h	

FEh	temperatureADC			This register is dual functioned. Reads module temperature ADC value. Writes data integrity value SerialEepromChecksum0.
Type	R/W	PoR	00h	

FFh	**vddADC**			**This register is dual functioned. Reads power supply, VDD ADC value. Writes data integrity value SerialEepromChecksum1.**
Type	**R/W**	**PoR**	**00h**	

7. Simplified Interface Models

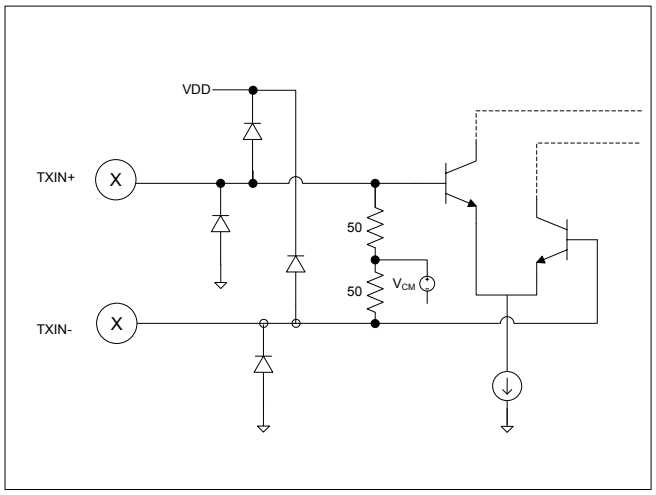


Figure 32- Transmit input structure

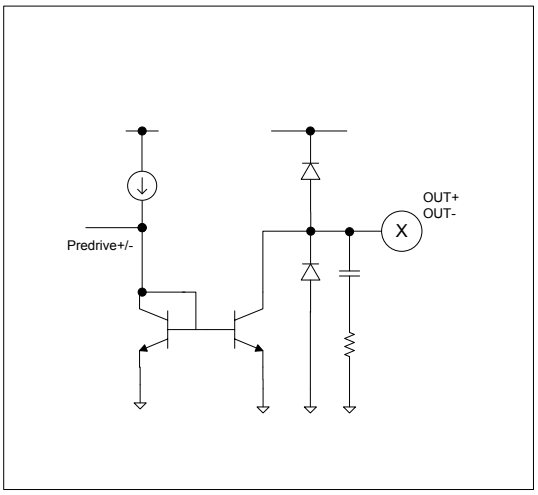


Figure 33- Transmit output structure

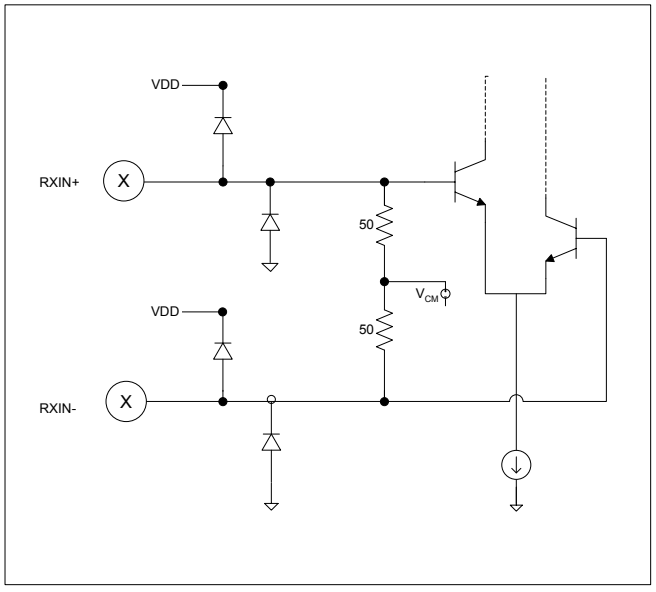


Figure 34- Receive input structure

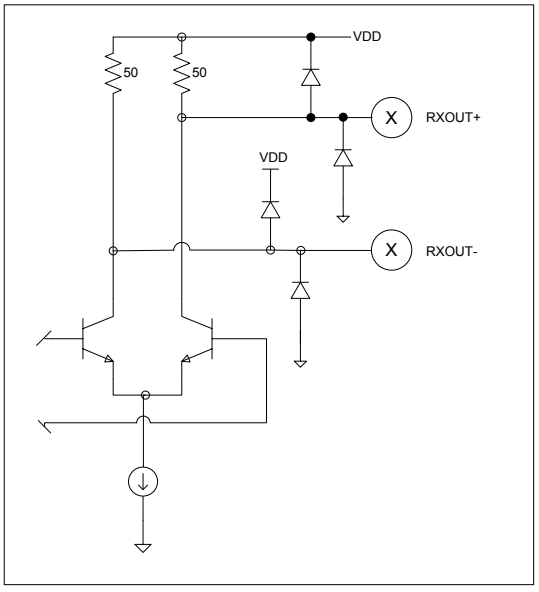


Figure 35- Receive output structure

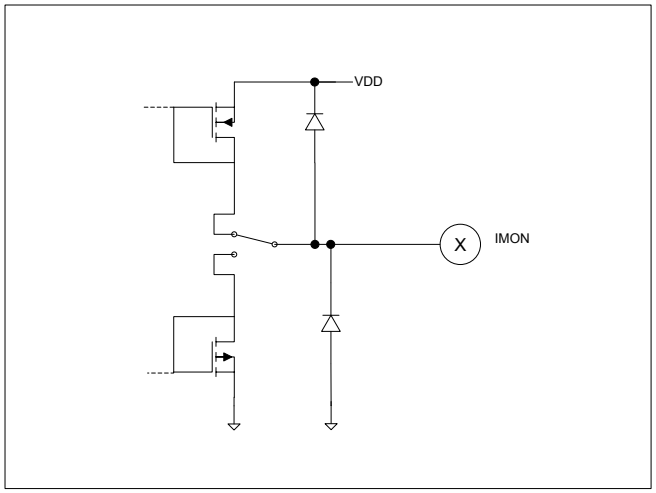


Figure 36- MPD input structure

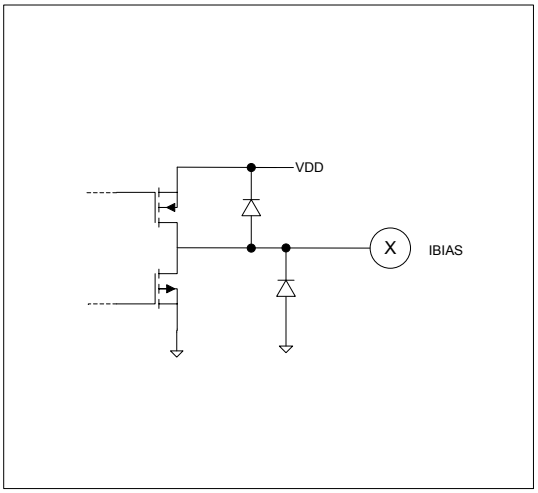


Figure 37- VCSEL bias output structure

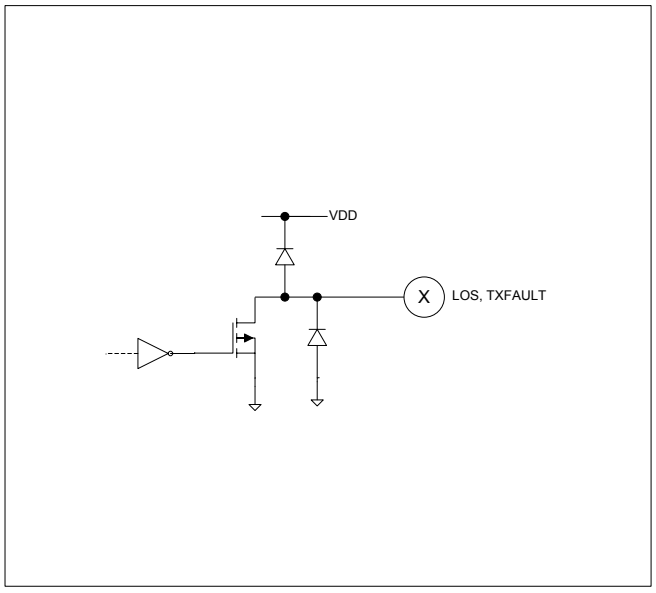


Figure 38- LOS/TX_FAULT output

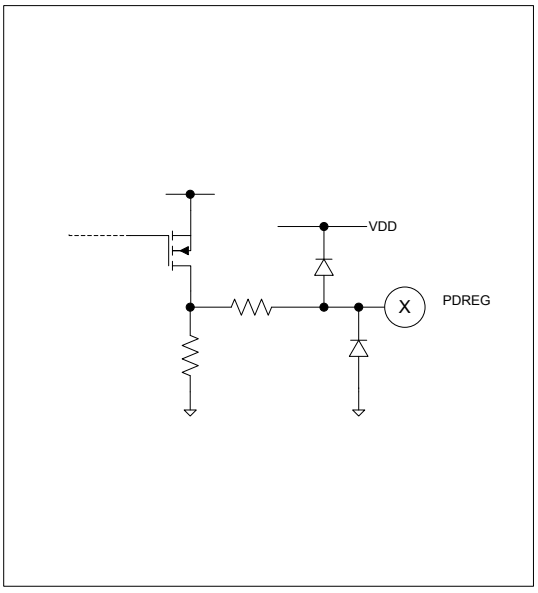


Figure 39- RSSI regulator output structure

8. Typical Applications

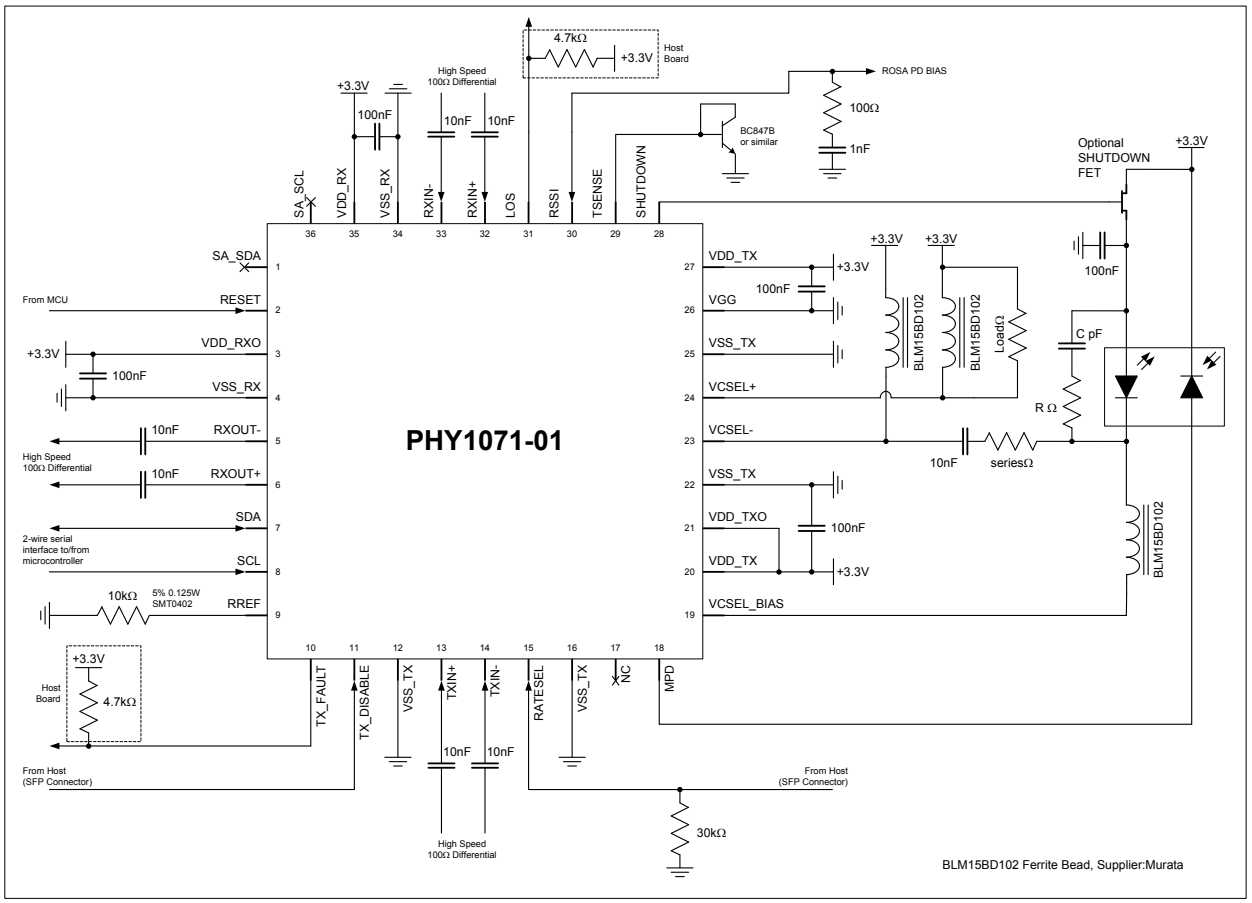


Figure 40 – PHY1071-01 in DDM Mode

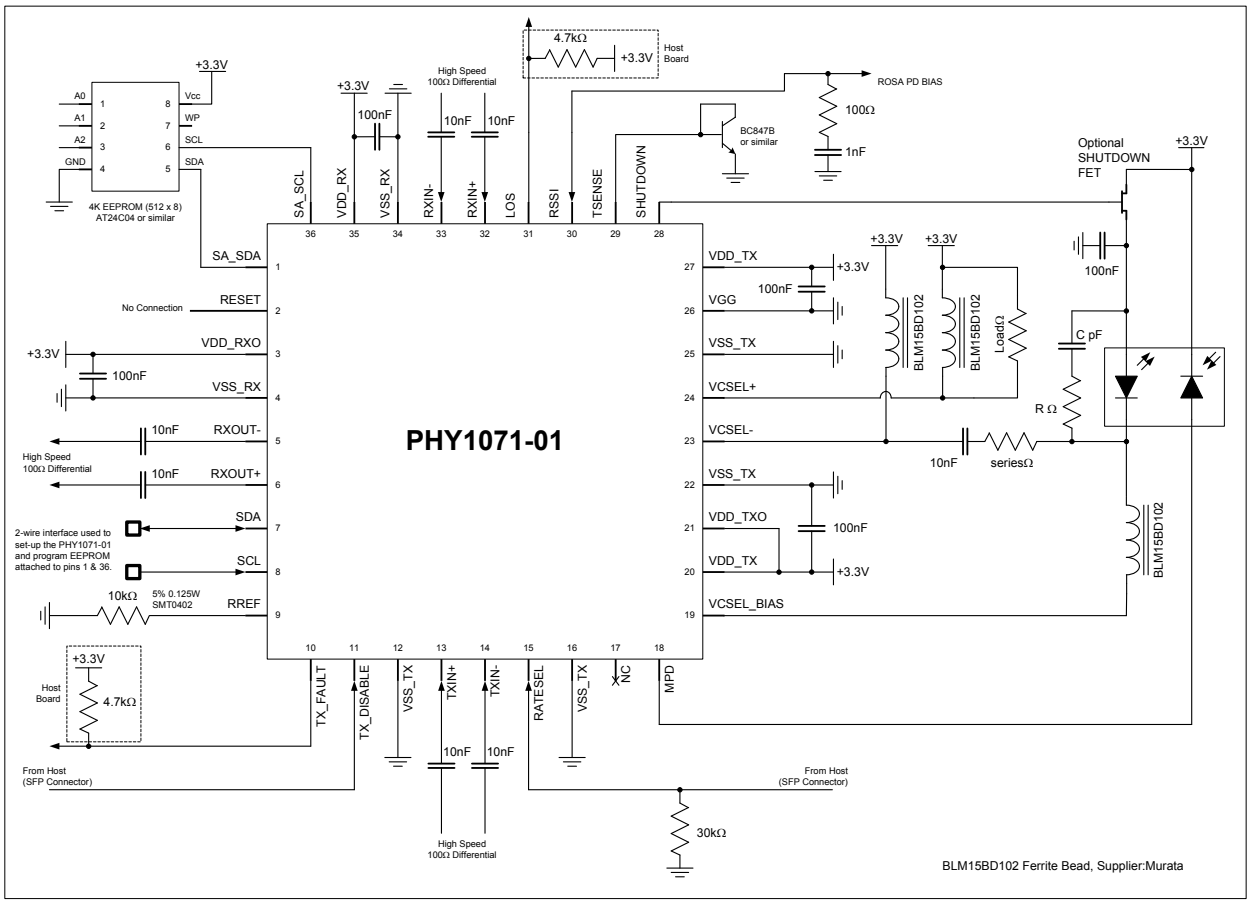


Figure 41 – PHY1071-01 in Stand Alone Mode

8.1. Power Supply Connections

The PHY1071-01 has been designed as a low power device. In order to achieve low operating power consumption the transmitter and receiver circuitry in the PHY1071-01 share some common internal bias circuitry. This requires that the PHY1071-01 transmitter and receiver be powered up together for correct operation. Powering up the transmitter VDDs and not the receiver VDDs, or the reverse, will not damage the PHY1071-01 but will cause the part to function incorrectly.

8.1.1. Power Supply Filtering

Although the Tx VDDs and Rx VDDs should be powered together and therefore, ultimately be connected at a common node, it is beneficial to separately filter the power supplies for the Tx VDD and Rx VDD supplies. Separately filtering the transmitter and receiver supplies off chip will reduce power supply noise and cross talk between the transmitter and receiver – it is generally good practice to separately filter and decouple the individual supplies on any multifunction IC.

In addition to supplying separately filtered supplies to the Tx VDDs and Rx VDDs of the PHY1071-01, it is also recommended that any other ICs and digital circuitry connected to the PHY1071-01 in an application environment (e.g. SFP module) be suitably filtered and decoupled also. An example of this would be to supply a filtered digital supply for the external MCU, required to compliment the PHY1071-01 in DDM SFF-8472 applications.

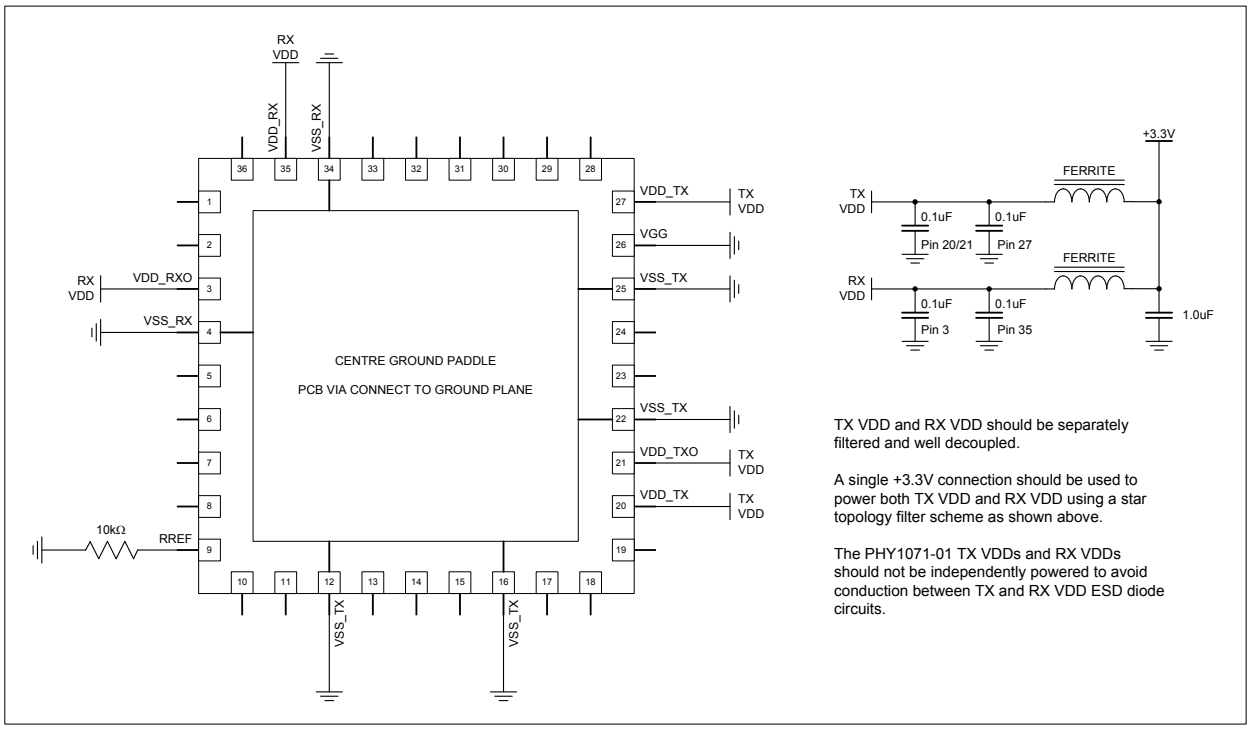
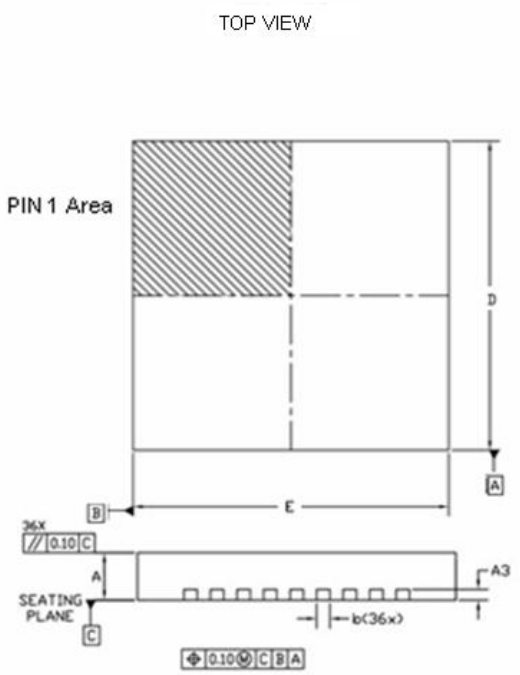


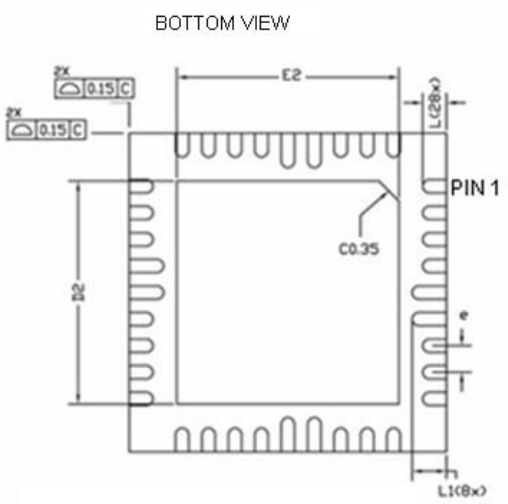
Figure 42 – Recommended power supply connections and filtering.

8.1.2. Power-On-Reset

The PHY1071-01 features an internal power-on-reset function that applies a reset to the internally digital logic once the supply voltage reaches a preset value (>2.0V). The internal power-on-reset typically takes 27ms after power has been applied based on a 50ms slow start voltage ramp. The PHY1071-01 may be reset externally by applying a logic high pulse to the reset pin. This is useful to guarantee the state of the PHY1071-01 logic when using the device in conjunction with an external MCU.

9. Packaging





Note:

1. Dimension and tolerancing conform to ASME Y14.5M-1994.
2. Controlling Dimensions: Millimeter, converted inch dimensions are not necessarily accurate
3. Dimension b applies to metallized terminal and is measured between 0.15 and 0.33mm from terminal tip.

Symbol	Common					
	Dimensions Millimeter			Dimensions Inch		
	Min	Nom	Max	Min	Nom	Max
A	See variation 'A'					
A3	0.203 Ref			0.008 Ref		
b	0.20	0.25	0.30	0.008	0.010	0.012
D	5.85	6.00	6.15	0.230	0.236	0.242
D2	4.10	4.20	4.30	0.161	0.165	0.170
E	5.85	6.00	6.15	0.230	0.236	0.242
E2	4.10	4.20	4.30	0.161	0.165	0.170
e	0.500 BSC			0.020 BSC		
L	0.40	0.45	0.50	0.016	0.018	0.020
L1	0.60	0.65	0.70	0.024	0.026	0.028

Package	Common					
	Dimensions Millimeter			Dimensions Inch		
	Min	Nom	Max	Min	Nom	Max
QFN	0.85	0.90	0.95	0.033	0.035	0.037
TQFN	0.70	0.75	0.80	0.027	0.029	0.031

Figure 41 - QFN 36 Package Outline Drawing

10. Contact Information

For technical support, contact Maxim at **www.maxim-ic.com/support**.

Disclaimer

This datasheet contains preliminary information and is subject to change.

The PHY1071-01 contains circuitry to aid the implementation of eye safety functions in equipment using laser devices. Phyworks Ltd accepts no liability for failure of this function in this product nor for injury to persons as a result of use of this product. Testing of the functionality of eye safety circuits in equipment using this product is the responsibility of the manufacturer of the equipment.

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